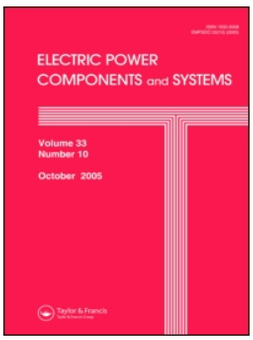

Taylor & Francis
Taylor & Francis Group

Electric Power Components and Systems

ISSN: 1532-5008 (Print) 1532-5016 (Online) Journal homepage: http://www.tandfonline.com/loi/uemp20

Proportional-Resonant and Slide Mode Control for Single-Phase UPS Inverter

Muhammad Aamir, Kafeel Ahmed Kalwar & Saad Mekhilef

To cite this article: Muhammad Aamir, Kafeel Ahmed Kalwar & Saad Mekhilef (2017) Proportional-Resonant and Slide Mode Control for Single-Phase UPS Inverter, Electric Power Components and Systems, 45:1, 11-21, DOI: 10.1080/15325008.2016.1233301

To link to this article: http://dx.doi.org/10.1080/15325008.2016.1233301

Electric Power Components and Systems, 45(1):11–21, 2017

ISSN: 1532-5008 print / 1532-5016 online
DOI: 10.1080/15325008.2016.1233301

Taylor & Francis
Taylor & Francis Group

Proportional-Resonant and Slide Mode Control for Single-Phase UPS Inverter

Muhammad Aamir, Kafeel Ahmed Kalwar, and Saad Mekhilef
Power Electronics and Renewable Energy Research Laboratory (PEARL), Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia

CONTENTS

Abstract—Slide mode control (SMC) is recognized as the most robust control with high stability, while the proportional-resonant (PR) control shapes the output waveform closely according to the reference sinusoidal signal. Keeping in view the characteristics of slide mode and PR control, a cascaded controller is proposed for bipolar single-phase uninterruptible power supply (UPS) inverter. The outer voltage loop uses the PR control while the inner loop uses the SMC. Chattering in the SMC has been removed using smoothed control law in narrow boundary layer condition. The stability of the controller has been analyzed using Lypunov stability criteria. The smoothed control law applied to the pulse width modulator results in fixed switching frequency of the inverter. The performance of the controller has been analyzed for single-phase inverter through simulations and experiments for both the linear and non-linear loads. The performance of controller has been compared with the other techniques of SMC and standard controllers. The proposed controller shows significant improvement in terms of reducing the total harmonics distortion to 0.5% for linear load and 1.25% for non-linear load, strong robustness, and fast response time of only 0.3 ms.

1. INTRODUCTION

Uninterruptible power supplies (UPSs) provide clean, conditioned, and regulated power to the varying load in all grid conditions. With the utilization of the rectifiers in the maximum critical loads like communications devices, medical equipment, and military equipment, it is mandatory to design UPS system with high-quality outputs. According to the IEEE standard 1547, minimum total harmonics distortion (THD) in the output voltage of UPS system should be maintained less than 5% for the nonlinear load [1–3].

Different high-performance control schemes have been presented for inverter control like deadbeat control [4], iterative learning control [5], model predictive control [6], and sliding mode control [7, 8]. Among these control schemes, deadbeat control [9] is the most popular control technique because of its fast dynamics response, as the tracking error settles to zero in finite sampling steps. However, the deadbeat control is very sensitive to model uncertainties, parameters mismatch, and

Keywords: slide mode control (SMC), proportional-resonant (PR) control, non-linear control, uninterruptible power supply (UPS), single-phase inverter, total harmonics distortion, chattering phenomena, Lypunov stability, robust control

Received 25 May 2015; accepted 24 August 2016

Address correspondence to Saad Mekhilef, Power Electronics and Renewable Energy Research Laboratory (PEARL), Department of Electrical Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia. E-mail: saad@um.edu.my

Color versions of one or more of the figures in the article can be found online at www.tandfonline.com/uemp.

noise in the high sampling frequency. Repetitive controller (RC) [10, 11] also provides good regulation for the non-linear loads with periodic distortions and excellent harmonics rejection. However, the dynamic response of the RC is relatively very slow, that is why another fast response control scheme is usually integrated with the RC to increase the response time of the controller. Moreover, poor tracking accuracy and large memory requirement are additional limitation in RC controller.

Alternatively for non-linear load, slide mode control (SMC) [12–14] strategy has gained special interest. SMC has been widely implemented in the power inverters because of its effective performance against non-linear system with uncertainties. A major feature of the SMC is its robustness, good dynamic response, stability against non-linear loading conditions, and easy implementation.

However, the SMC has the inherit drawback of chattering phenomena because of the variable switching frequency which cause low control accuracy, high power losses, and complication in the filter design. In order to eliminate chattering, SMC has been implemented with fixed switching frequency variable width hysteresis comparator [15], and quasi-sliding control based on zero-average dynamic (ZAD) [16]. Chattering problem can also be eliminated by smoothing the control discontinuous in a thin boundary layer neighboring the switching surface [17].

Integral SMC method has been proposed for efficient AC tracking of the system in [18, 19]. Although this system has reduced the harmonics contents in output voltage, it has limited ability for high-order harmonics. Slide mode control with continuous-time control method has been implemented in [20, 21]. But the filter inductor's current has been used as a state variable, which requires complex computation for its reference function. Also, the SMC operates at variable switching frequency, which leads to undesirable chattering phenomena. Hysteresis-type switching function has been introduced for each leg of the inverter, which increases the hardware complexity [22]. In rotating SMC [23], time-varying slope based on SMC method was proposed, which rotate the sliding surface in order to get the faster response for the non-linear conditions. This different value for the slope has been applied during the transient- and steady-state operation, causing the surface to rotate according to load variation. SMC with proportional integral (PI) controller has been implemented in [24]. Although PI controller provides an infinite gain with a constant variable and step reference without steady-state error, it is unable to track a sinusoidal reference. Hence, its performance for inverter control is not satisfactory.

Proportional-resonant (PR) controller can achieve tight sinusoidal reference tracking for the voltage source inverter, by providing large gain at the resonance frequency, thus eliminating the steady-state error and improving the system performance. With the motivation to analyze the performance of the SMC and PR controller in the inverter, a cascaded control algorithm of SMC and PR control has been proposed in this paper. It is a new control scheme for the single-phase bipolar voltage source inverter for UPS application. The inner current loop is controlled by the SMC because it provides the robust control of the capacitor current, which has high harmonics for the nonlinear loading condition. While the outer voltage loop is controlled by the PR control, it tightly tracks the sinusoidal reference voltage resulting in better voltage regulation. Hence, PR can be used for implementing selective harmonic compensation without requiring excessive computational resources. The chattering phenomenon in the SMC is eliminated by using smoothed control law in narrow boundary layer. The smoothed control law applied to the pulse width modulator results in the fixed switching frequency of the inverter. Thus, the proposed controller adopted the characteristic of both SMC and PR control. The controller shows good response with low THD and high stability for non-linear loads. The main advantages of the proposed controller are as follows:

1. very low THD for both linear and non-linear load;
2. very robust in operation;
3. fast transient response; and
4. easy implementation.

The paper is organized as follows: The system modeling of the inverter is presented in Section 2, while the SMC and PR controls are explained in Sections 3 and 4, respectively. The simulation and experimental results are discussed in Sections 5 and 6, respectively. Finally, the conclusions of this work are presented in Section 7.

2. SYSTEM MODELING

The circuit diagram of single-phase inverter for the UPS system with LC filter is shown in Figure 1, where V_{DC} is applied voltage and V_{out} is the filter capacitor C output voltage. i_{L} is the inductor L current and i_{O} is the output current through the load R, given by $i_{\mathrm{O}} = V_{\mathrm{out}}/\mathrm{R}_{\mathrm{Load}}$. The state equations of the inverter are given as

$$L\frac{di_L}{dt} = uV_{\mathrm{DC}} - V_{\mathrm{out}} \tag{1}$$

$$C\frac{dV_{\mathrm{out}}}{dt} = i_c = i_L - i_o \tag{2}$$

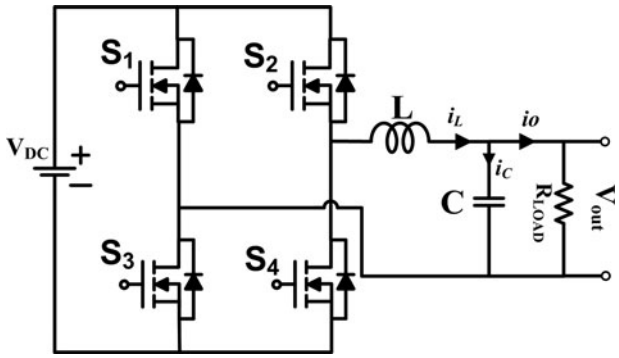

FIGURE 1. Single-phase inverter for UPS system.

The behavior of the system can be represented by the following state-space equation:

$$\frac{d}{dt}\begin{bmatrix} V_{\text{out}} \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & {}^{1}\!/_{C} \\ -{}^{1}\!/_{L} & 0 \end{bmatrix}\begin{bmatrix} V_{\text{out}} \\ i_L \end{bmatrix} + \begin{bmatrix} 0 \\ {}^{V_{DC}}\!/_{L} \end{bmatrix} u + \begin{bmatrix} -{}^{i_o}\!/_{C} \\ 0 \end{bmatrix} \tag{3}$$

where $u = \text{Controlinput} = \{-1, 0, 1\}$

In order to implement the SMC, the voltage error x_1 and its derivative $x_2 = \dot{x}_1$ need to be found

$$x_1 = V_{\text{out}} - V_{\text{ref}} \tag{4a}$$

$$x_2 = \dot{x}_1 = \dot{V}_{\text{out}} - \dot{V}_{\text{ref}} = {}^{i_C}\!/_{C} - \dot{V}_{\text{ref}} \tag{4b}$$

where $V_{\text{ref}} = V_m \sin(\omega t)$

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -{}^{1}\!/_{LC} & -{}^{1}\!/_{RC} \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ {}^{V_{\text{DC}}}\!/_{LC} \end{bmatrix} u + \begin{bmatrix} 0 \\ -{}^{V_{\text{ref}}}\!/_{LC} \end{bmatrix} \tag{5}$$

3. SLIDING MODE CONTROL

Slide mode control (SMC) is a non-linear control method, which changes the dynamics of the system by employing the discontinuous control signal that forces the system to slide along the system normal behavior. According to the SMC theory, a control has to be designed, which will direct the state trajectory toward the zero sliding surface. The sliding control law is given as

$$u(t) = \begin{cases} \neq 1, & \text{if } S(x) > 0 \\ -1, & \text{if } S(x) < 0 \end{cases} \tag{6}$$

where *S(x)* is called sliding surface and normal system behavior has $S(x) = 0$. The linear sliding surface function can be expressed as:

$$S = \lambda x_1 + x_2, \quad \lambda 0 \tag{7}$$

where λ is a real constant. For the dynamic behavior, Eq. (7) will be

$$S = \lambda x_1 + \dot{x}_1 = 0 \tag{8}$$

The objective of the control in Eq. (7) is to drive the trajectory of the system from any initial condition $x(0)$ to the sliding surface $S(x) = 0$. This trajectory is maintained at the sliding surface, and consequently directs the system toward the steady-state condition. Thus, the SMC performs its control by utilizing the sliding surface as a reference and thus satisfies the inequality condition

$$\lim_{s\to 0\neq} \frac{d(s)}{dt} 0 \text{ and } \lim_{s\to 0^-} \frac{d(s)}{dt} 0$$

In order to ensure the stability of the sliding function, the Lyapunov function $V(t) = S^2/2$ has to be satisfied with the minimum condition $\dot{V}(t)\,\eta\,|s|$, keeping the scalar s at zero while η is strictly positive constant [12, 25]. Hence, the condition for stability will be $\dot{V}(t) < 0$.

$$\dot{V}(t) = S\dot{S} \tag{9}$$

$$\dot{V}(t) = S[\lambda \dot{x}_1 + \dot{x}_2] \tag{10}$$

$$\dot{V} = S\left[\lambda x_2 - \frac{1}{LC}x_1 + \frac{V_{\text{DC}}}{LC}u - \frac{V\text{ref}}{LC} - \frac{x_2}{RC}\right] \tag{11}$$

Consider the discrete control law as follows:

$$u(t) = \text{sign}(s) = \begin{cases} \neq 1, & \text{if } S(x) > 0 \\ -1, & \text{if } S(x) < 0 \end{cases} \tag{12}$$

In order to satisfy the sliding condition (9), despite the uncertainty on the dynamics of the non-linear function, u is replaced by the –sign(*s*), where "sign" is the sign function.

$$\dot{V}S\left[\lambda x_2 - \frac{1}{LC}x_1 - \frac{V_{\text{DC}}}{LC}\text{sign}(s) - \frac{V\text{ref}}{LC} - \frac{x_2}{RC}\right] \tag{13}$$

$$\dot{V}|S|\left[\text{sign}(x)\left[\lambda x_2 - \frac{1}{LC}x_1 - \frac{V\text{ref}}{LC} - \frac{x_2}{RC}\right]\right] - \frac{V_{\text{DC}}}{LC} \tag{14}$$

$$\text{sign}(x)\left[\lambda x_2 - \frac{1}{LC}x_1 - \frac{V\text{ref}}{LC} - \frac{x_2}{RC}\right] < \frac{V_{\text{DC}}}{LC} \tag{15}$$

Hence, it is clear that the stability condition is fulfilled when Eq. (15) is satisfied.

Putting the value of voltage and current error in Eq. (7) provides the sliding control law of the inverter

$$S = \lambda(V_{\text{out}} - V_{\text{ref}}) + \frac{i_C}{C} - \dot{V}_{\text{ref}} \tag{16}$$

Although the implementing of SMC involves the derivative of the voltage error, it is well known that the differential operation amplifies high-frequency components in a signal. Therefore, capacitor current feedback is used to avoid the derivative operation in creating the sliding function [22]. Hence, the state variable x_2 can be obtained as $x_2 = \dot{x}_1 = \frac{1}{C}(i_C - i_{\text{ref}})$, where $i_{\text{ref}} = C\dot{V}_{\text{ref}}$ is the reference for the capacitor current

$$S = \lambda (V_{\text{out}} - V_{\text{ref}}) + \frac{1}{C}(i_C - i_{\text{ref}}) \tag{17}$$

Since the sliding mode controller has the common inherent property of chattering phenomena, it causes low control accuracy and high losses in the circuit. In order to overcome the chattering phenomena, a smoothed SMC has been implemented. This can be achieved by smoothing out the control discontinuity in a thin boundary layer neighboring the sliding surface.

$$B(t) = \{x, |S(x;t)| \leq \emptyset\} \emptyset > 0 \tag{18}$$

where $\emptyset$ is the boundary layer thickness and $\omega = \frac{\phi}{\lambda}$ is the boundary layer width. Hence, $B(t)$ is chosen such that all the trajectories starting at $B(t > 0)$ remain inside the $B(t)$ for all t > 0. Hence we interpolate S inside $B(t)$ for instance, and replace S by an expression S/$\emptyset$. Thus, Eq. (17) will be

$$\frac{S(x)}{\emptyset} = \frac{\lambda}{\emptyset}[V_{\text{out}} - V_{\text{ref}}] + \frac{1}{C\emptyset}[i_C - i_{\text{ref}}] \tag{19}$$

The closed-loop control of the inverter as shown in Figure 2 is obtained from the previous description of the SMC. G_{INV} is the model of the inverter with low-pass LC filter employed at the output of the inverter. The SMC block represents the implementation of Eq. (19), where V_{ref} is the reference voltage that is compared with the output voltage across the filter capacitor C. The voltage error multiplied with λ/α is considered as reference current, and is fed to the inner current loop. The reference current is compared with the feedback capacitor current i_C, and current error multiplied with $\emptyset$ is provided to the pulse width modulation (PWM) modulator.

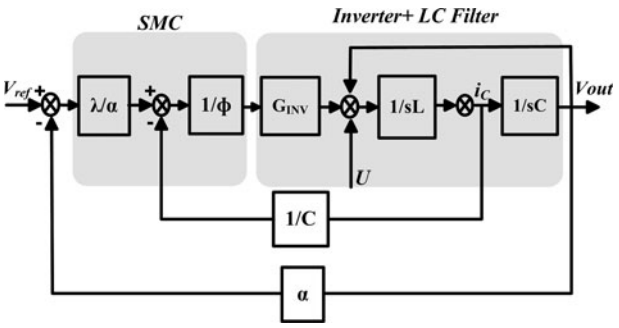

FIGURE 2. Block diagram of the SMC with inverter and LC filter.

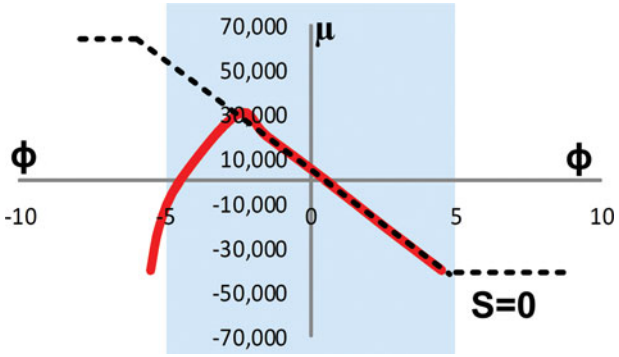

FIGURE 3. Control interpolation in boundary layer.

The smoothing control discontinuity assigns a low-pass filter structure to the local dynamics, thus eliminating chattering. The control law needs to be tuned very precisely in order to achieve a trade-off between the tracking precision and robustness to the uncontrolled dynamics as shown in Figure 3.

4. PROPORTIONAL-RESONANT CONTROL

Conventionally, the PR controller provides a large gain at the fundamental frequency and strictly follows the sinusoidal reference, reducing the steady-state error and improving the stability of the system. The transfer function of the ideal PR controller is given by Eq. (20):

$$G_{PR} = K_P + \frac{2K_R s}{s^2 + \omega_o^2} \tag{20}$$

where K_P is the proportional gain, ω_0 is the resonant frequency, and K_R is the resonant gain. The ideal PR controller gives infinite gain at the resonant frequency but no gain and phase shift at other frequencies. In order to avoid stability problem associated with infinite gain, more appropriate non-ideal PR controller is used, as shown in Eq. (21):

$$G_{PR} = K_P + \frac{2K_R \omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \tag{21}$$

Hence selecting a suitable cut-off frequency ω_c can widen the bandwidth, reducing the sensitivity toward the frequency variations. By combining the PR controller with the SMC, the performance of the inverter is improved, as the resonance controller provides better regulation of the output voltage and reduces the total harmonic distortion considerably [26, 27].

The block diagram of SMC with PR controller is shown in Figure 4. G_{PR} is the model of the PR controller introduced in the voltage loop of the controller. This increases the performance by precisely tracking the reference AC voltage. The current loop is controlled by the previously described SMC (Figure 2). In proposed controller, both the PR and SMC work

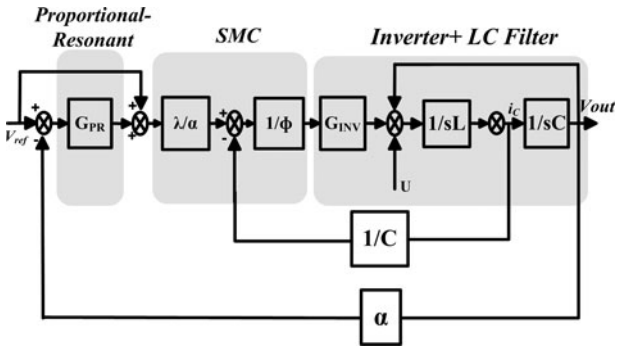

FIGURE 4. Equivalent control diagram with SMC and PR control.

are cascaded to control the inverter of the UPS system. The open-loop gain of the voltage control loop with the PR compensator can be obtained by Eq. (22):

$$H(s) = G_{PR}G_{INV} = \left(K_P + \frac{2K_R\omega_c s}{s^2+2\omega_c s+\omega_o^2}\right) \times \left(\frac{sCr_d+1}{LCs^2+sCr_d+1}\right) \tag{22}$$

$$H(s) = \frac{a_3s^3+a_2s^2+a_1s+a_0}{b_4s^4+b_3s^3+b_2s^2+b_1s+b_0} \tag{23}$$

where

$$a_3 = K_pCr_d,\ a_2 = K_p + 2\omega_cCr_d(K_r+K_p),\ a_1 = 2K_p\omega_c + 2K_r\omega_c + K_pCr_d\omega_0^2,\ a_0 = K_p\omega_0^2$$

$$b_4 = LC,\ b_3 = 2\omega_cLC + Cr_d,\ b_2 = LC\omega_0^2 + 2Cr_d\omega_c + 1,$$

$$b_1 = Cr_d\omega_0^2 + 2\omega_c,\ b_0 = \omega_0^2$$

The Bode plot of the voltage loop is shown in Figure 5. It can be seen from the compensated voltage loop gain that the large system bandwidth would give the voltage controller a fast response. Meanwhile, having a phase margin of 2° demonstrates closed-loop stability. However, as can be seen from the Bode plot in Figure 5, the phase margin is very low, which may affect the output voltage by inserting the unwanted oscillations. This can be compensated by adding a suitable lead–lag compensator as shown in Figure 6.

$$G_{\text{lead-lag}}\frac{1+as}{1+bs} \tag{24}$$

where $b = x * a$, and x is the ratio that can be calculated as $(1-\sin\ \emptyset)/(1+\sin\emptyset)$, and Ø is the required phase margin. Thus, the lead–lag compensator improves the phase margin of the voltage loop by reducing the steady-state error to almost

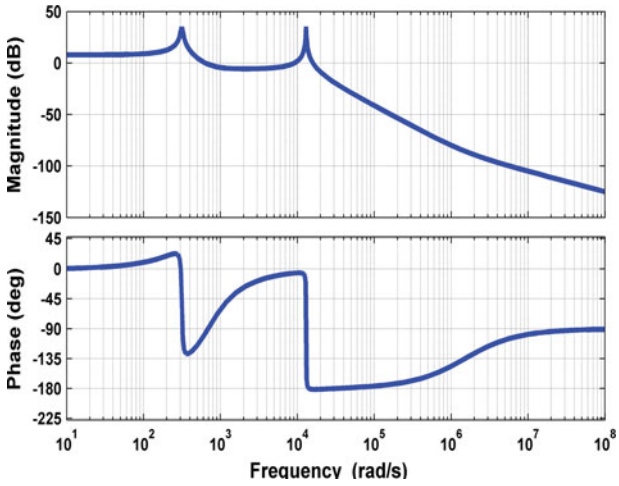

FIGURE 5. Bode plot of voltage loop with PR controller.

zero for harmonic components. Figure 6(b) shows the Bode plot of the outer voltage loop with lead–lag compensator. The phase margin of the loop is improved to 78° – quite high which leads to oscillating free output of the system.

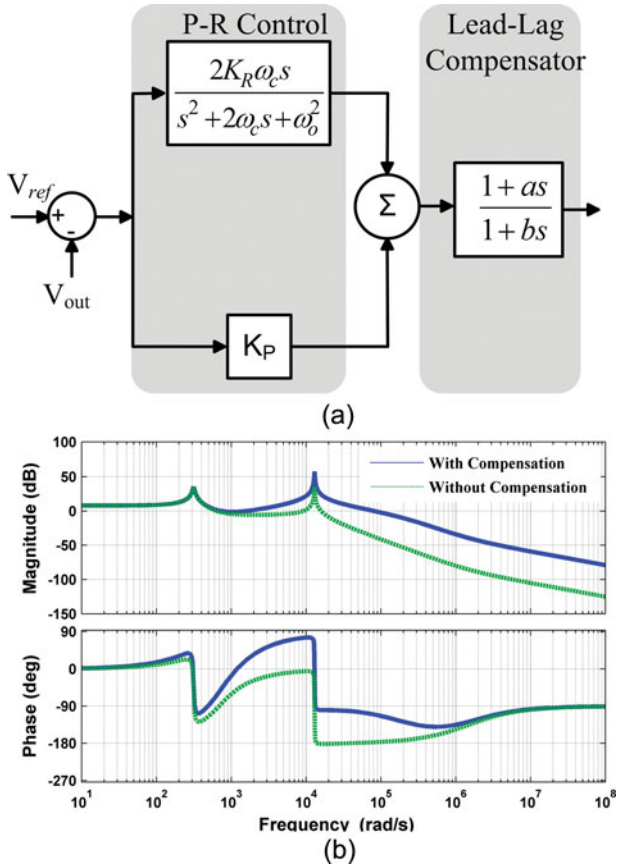

FIGURE 6. Lead–lag compensator with PR controller. (a) PR control with lead–lag compensator. (b) Bode plot of voltage loop.

Hence, the slide surface with the PR control can be presented as Eq. (25):

$$\frac{S(x)}{\emptyset} = \frac{1}{C\emptyset}\left[i_C - i_{\text{ref}}\right] + \frac{\lambda}{\emptyset}\left[K_p\left(V_{\text{out}} - V_{\text{ref}}\right) + k_i\left(\frac{2s}{s^2 + 2\omega_c s + \omega_o^2}\right)\left(V_{\text{out}} - V_{\text{ref}}\right)\right] \quad (25)$$

Thus, Eq. (25) shows the dynamic behavior of the system with both SMC and PR compensator. The error in the voltage loop is compensated by the appropriate PR parameters, thus the output voltage is compelled to follow the reference AC voltage leading to the system stability, while the SMC drive the system to the zero sliding surface with maximum stability. Since the capacitor error current contains the ripples from the inductor, the current peak may reach high values. So Ø should be carefully assigned values in order to compensate the slope from the high current ripple of the capacitor. Hence, the PR controller eliminates the steady-state error at resonant frequency or harmonic at that frequency.

Now the condition of stability is modified as

$$|s| \geq \emptyset \Rightarrow \frac{1}{2}\frac{d}{dt}S^2 \leq \left(\dot{\emptyset} - \eta\right)|s| \quad (26)$$

The $\dot{\emptyset}\,|s|$ illustrates the fact that the boundary layer attraction condition shows more firmness during boundary layer contraction ($\dot{\emptyset} < 0$) and less firmness during boundary layer expansion ($\dot{\emptyset} > 0$).

The response time of the system λ determines the dynamics and robustness of the system. It is clear from Eq. (25) that smaller value of λ leads to slow response time, while higher λ values increase the response time but take larger time to reach the sliding surface. Thus, the optimal value for λis equal to the switching frequency of the inverter.

According to [28], in order to maintain proper control over the capacitor current, multiple crossing between the error signal from the current loop and the triangular waveform must be avoided. Hence, the maximum slope of the error signal should be less than the slope of the triangular waveform (carrier). This means that the following condition applies in terms of magnitudes

Slope of error signal < Slope of the carrier signal

The slope of the carrier wave is$4V_m \times fs$, where $V_m$is the magnitude of the carrier signal and*fs* is the frequency of carrier signal. The slope of the error signal to the modulator is given by$V_{\text{DC}}/4LC\emptyset$. According to the limitation of the pulse width modulator,

$$4V_m \times fs \gg {}^{V_{\text{DC}}}/_{4LC\emptyset} \quad (27)$$

Circuit parameter	Value
Input voltage	180 V_{DC}
Output voltage	110 V_{AC}
Output power	400 W
Inductor	840 μH
Capacitor	6.6 μF
Switching frequency	20,000 Hz

TABLE 1. Circuit specifications

$$\emptyset \gg \frac{V_{\text{DC}}}{16LCV_m f_S} \quad (28)$$

Considering the limitation of the PWM modulator, the minimum approximate value of Ø can be calculated using the equation:

$$\emptyset \cong \frac{10V_{\text{DC}}}{16LCV_m f_S} \quad (29)$$

5. SIMULATION

The performance of the proposed control has been verified by simulation using MATLAB (The MathWorks, Natick, Massachusetts, USA)/Simulink. The circuit specifications are given in Table 1, and control parameters are listed in Table 2. K_p and K_R are the proportional gain and resonant gain selected for stable response of the PR controller from Eq. (22). The value of α is the division factor to bring the output voltage comparable to reference and is selected considering the electronic circuit limitations. λ is the dynamic response of the inverter, and is equal to the switching frequency of the modulator, whereas Ø is calculated using Eq. (29). Magnitude of the carrier (V_m) is selected to realize the inequality (27). The steady-state load tests have been performed using linear and non-linear single-phase uncontrolled diode rectifier. The reference non-linear load has been designed according to the standard of IEC62040-3 [1], with input series resistance of 0.3 Ω [4% of (output rms voltage)^2/apparent power], parallel load resistance of 30 Ω [rectified voltage/(60% of apparent

K_P	2.5
K_R	30
λ	20,000
Φ	126,830
V_m	8 V
α	0.045454
V_{ref}	110V_{AC}

TABLE 2. Controller parameters

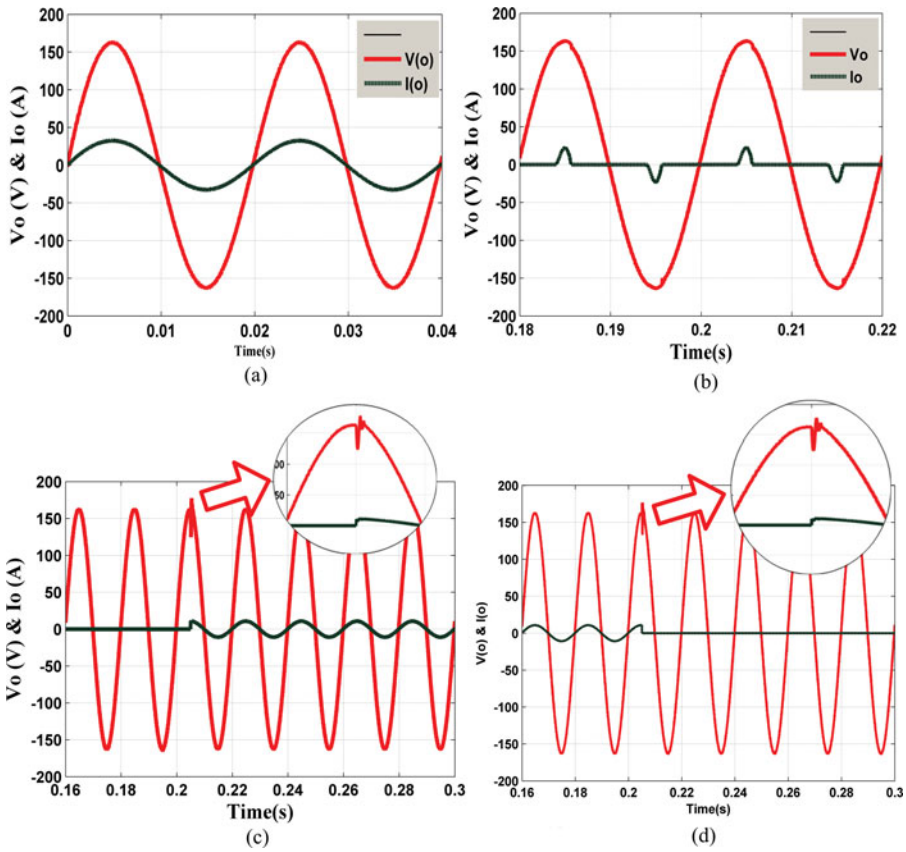

FIGURE 7. Simulation waveform of output voltage and current. (a) Linear load. (b) Non-linear load. (c) Step response from 0 to 100%. (d) Step response from 100 to 0%.

power)], and filter capacitor C = 4700 μF [7.5/(output frequency × load resistance)]. The results are evaluated using the transient response, steady-state error, and THD for both linear and non-linear loads. Figure 7(a) shows the output voltage and current waveform of the inverter for both linear and non-linear loads. Considering the controller parameter, the THD measured for the linear and non-linear load is 0.45 and 1.25%, respectively, which is considerable low as compared to other control schemes. Figure 7(c) shows the output voltage during step change in load from 0 to 100%, and back from 100 to 0%. The controller shows satisfactory performance with only 0.3 ms of settling time.

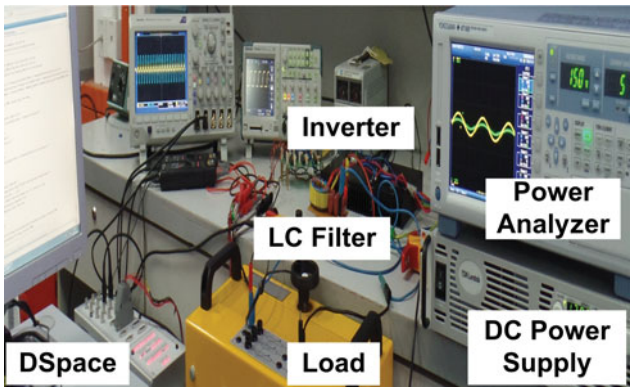

FIGURE 8. Photograph of experimental prototype.

6. EXPERIMENTAL RESULTS

A 400-W experimental prototype, shown in Figure 8, has been built in order to validate the performance of the proposed controller. The controller was implemented with DS1104 Slave I/O PWM. The performance of the controller is examined for both linear and non-linear uncontrolled diode rectifier loads.

6.1. Steady-state Performance

The output voltage and current waveform for both linear and non-linear loads are shown in Figure 9. The THD of the out-

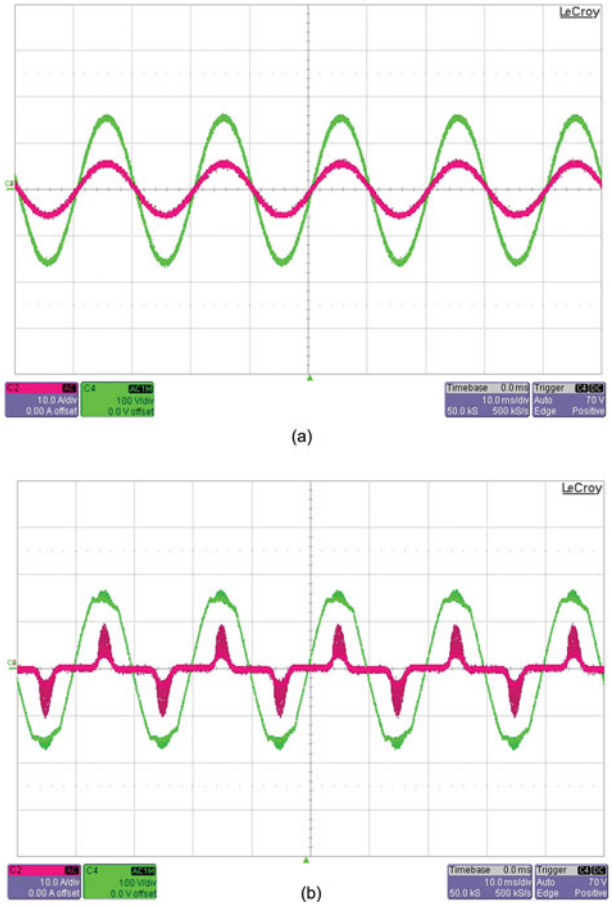

FIGURE 9. Experimental waveform of output voltage and current. (a) Linear load, voltage scale 100 V/div, current 10 A/div, time 10 ms/div. (b) Non-linear load, voltage scale 100 V/div, current 10 A/div, time 10 ms/div.

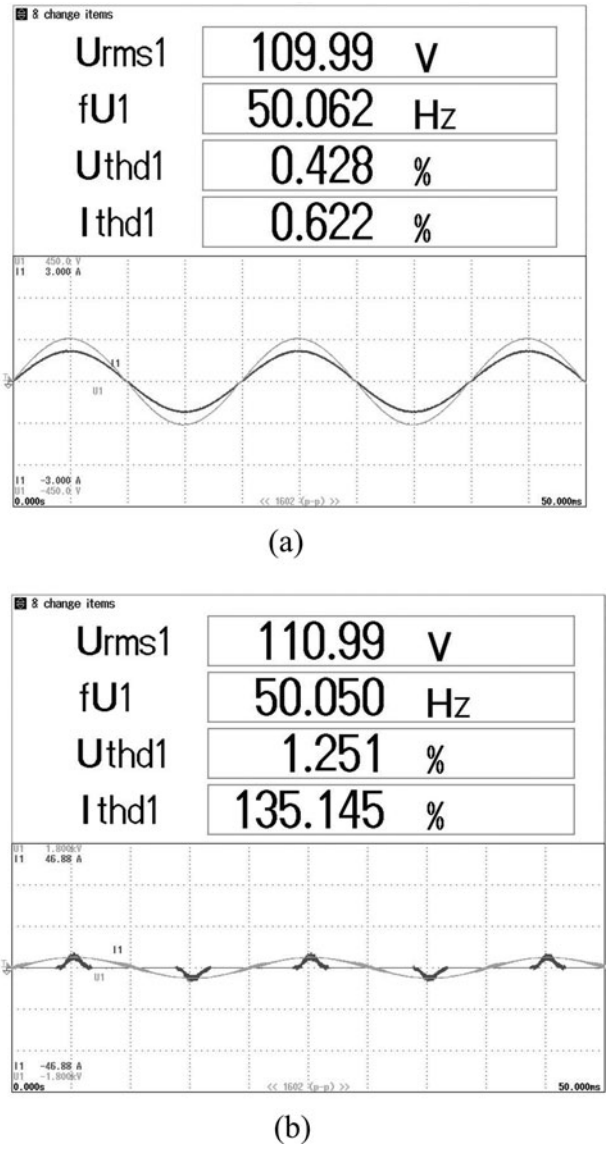

FIGURE 10. THD of output voltage and current with power analyzer. (a) Liner load. (b) Non-linear load.

put voltage is about 0.45%, similar to the results obtained in simulation. Similarly, the THD of the output voltage is only 1.25% for non-linear load. It can be seen from these results that the THD of the output voltage is very low even for severe operating condition. The crest factor of the output voltage for the non-linear load is 1.7. The THD of the UPS output voltages shown in Figure 10 are well below the limits of IEC 62040-3. The THD measurements given in this paper are taken by Yokogawa WT1800 Precision Power Analyzer. Figure 11 shows the comparison of the THD between SMC and PR + SMC. There is significant improvement in the THD for the cascaded PR and SMS controller, with the reduction of the THD to about 0.8% for linear load and 0.6% for non-linear loads.

6.2. Transient Performance

In order to verify the transient performance of the UPS system, the standard tests have been carried out. Figure 12(a) shows the experimental waveform of the step change in load from 100 to 0%, while Figure 12(b) shows the experimental waveform of step change from 0 to 100%. The settling time in both the case is less than 0.3 ms. The experimental results show that the dynamic behavior of the controller is satisfactory and does not exceed the classification 1 of IEC62040-3 standard [29]. Thus, this UPS is suitable for the applications when high-quality output voltage is required for critical loading condition. Table 3 shows the comparison of the proposed work with the SMC and other common controllers. The proposed controller shows an improvement in terms of reducing the THD and transient response with robust control of the inverter.

Controllers	Deadbeat [4]	Iterative learning [5]	Model predictive control [6]	SPWM control [30]	Rotating SMC [23]	Fix-Freq SMC [31]	Proposed work
V_{DC}	600	150	529	405	300	360	180
V_{RMS}	220	110	150	220	200	220	110
Filter capacitor (uF)	15	117.1	40	202	100	9.4	6.6
Filter inductor(mH)	1.2	0.58	2.4	0.03	0.250	0.357	0.84
THD (L) (%)	2.8	1.27	2.85	1.11	–	1.1	0.45
THD (NL) (%)	4.1	1.33	3.8	3.8	2.66	1.7	1.25
Response time (ms)	0.5	–	50	60	–	0.5	0.3

TABLE 3. Comparison of different control methods

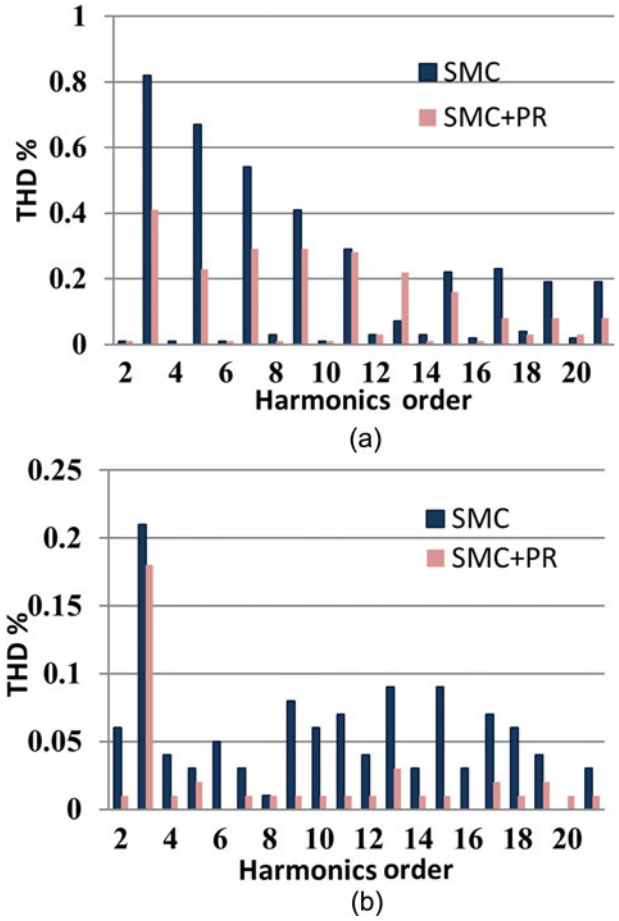

FIGURE 11. Comparison of THD between SMC and SMC + PR. (a) Linear load (for SMC THD = 1.1%), (SMC + PR THD = 0.5%). (b) Non-linear load (for SMC THD = 2.1%), (SMC + PR THD = 1.25%).

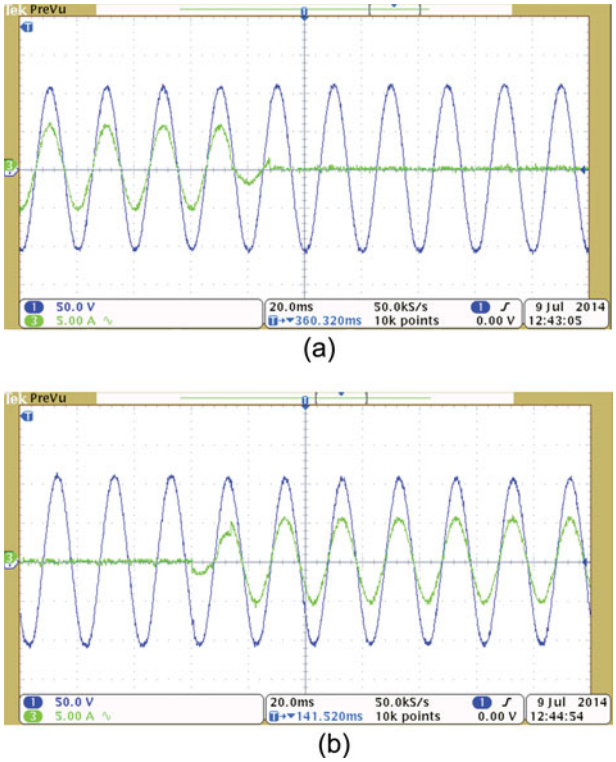

FIGURE 12. Step change in output voltage and current. (a) 100 to 0%, voltage scale 50 V/div, current 5 A/div, time 20 ms/div. (b) 0 to 100%, voltage scale 50 V/div, current 5 A/div, time 20 ms/div.

7. CONCLUSION

A single-phase UPS inverter with a SMC cascaded with PR controller has been introduced in this paper. The chattering problem in the SMC has been reduced using smoothed control law in narrow boundary layer. The PR compensator controls the fundamental frequency and the output voltage, while the

SMC performs robust control of the inverter. The performance of the control has been analyzed through simulation results and experimental prototype. The steady-state output voltage has high quality under both linear and non-linear loads with low THD and fast transient response. The output voltage dynamics response of the UPS inverter is found to be very good, meeting the Class 1 of IEC64020-3, standard for linear and non-linear load. As a perspective for future work, the proposed design worked can be extended for the control of three-phase UPS inverter.

FUNDING

The authors gratefully acknowledge the support of the University of Malaya Post-graduate Research Grant (PPP), project no. PG187-2015B.

REFERENCES

[1] "Uninterruptible power systems (UPS)—Part 3: Method of specifying the performance and test requirements," First Edition 1999-03, International Standard IEC 62040-3.

[2] Marei, M. I., Abdallah, I., and Ashour, H., "Transformerless uninterruptible power supply with reduced power device count," Electr. Power Compon. Syst., Vol. 39, No. 11, pp. 1097–1116, July 2011.

[3] Nasiri, A., Amac, A., and Emadi, A., "Series-parallel active filter/uninterruptible power supply system," *Electr. Power Compon. Syst.*, Vol. 32, No. 11, pp. 1151–1163, November 2004.

[4] Mattavelli, P., "An improved deadbeat control for UPS using disturbance observers," *IEEE Trans. Ind. Electron.*, Vol. 52, No. 1, pp. 206–212, February 2005.

[5] Deng, H., Oruganti, R., and Srinivasan, D., "Analysis and design of iterative learning control strategies for UPS inverters," *IEEE Trans. Ind. Electron.*, Vol. 54, No. 3, pp. 1739–1751, June 2007.

[6] Cortes, P., Ortiz, G., Yuz, J. I., Rodriguez, J., Vazquez, S., and Franquelo, L. G., "Model predictive control of an inverter with output filter for UPS applications," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 6, pp.1875–1883, June 2009.

[7] Tai, T., and Chen, J., "UPS inverter design using discrete-time sliding-mode control scheme," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 1, pp. 67–75, February 2002.

[8] Hu, J., Shang, L., He, Y., and Zhu, Z. Q., "Direct active and reactive power regulation of grid-connected DC/AC converters using sliding mode control approach," *IEEE Trans. Power Electron.*, Vol. 26, No. 1, pp. 210–222, January 2011.

[9] Benyoucef, A., Kara, K., Chouder, A., and Silvestre, S., "Prediction-based deadbeat control for grid-connected inverter with L-filter and LCL-filter," *Electr. Power Compon. Syst.*, Vol. 42, No. 12, pp. 1266–1277, September 2014.

[10] Zhang, K., Kang, Y., Xiong, J., and Chen, J., "Direct repetitive control of SPWM inverter for UPS purpose," *IEEE Trans. Power Electron.*, Vol. 18, No. 3, pp. 784–792, May 2003.

[11] Rech, C., Pinheiro, H., Gründling, H. A., Leaes, H., and Pinheiro, J. R., "A modified discrete control law for UPS applications," *IEEE Trans. Power Electron.*, Vol. 18, No. 5, pp. 1138–1145, September 2003.

[12] Yan, W., Hu, J., Utkin, V., and Xu, L., "Sliding mode pulse width modulation," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, pp. 619–626, March 2008.

[13] Schirone, L., Celani, F., and Macellari, M., " Discrete-time control for DC-AC converters based on sliding mode design," *IET Power Electron*., Vol. 5, No. 6, pp. 833–840, July 2012.

[14] Navarro-Lopez, E. M., Cortes, D., and Castro, C., "Design of practical sliding-mode controllers with constant switching frequency for power converters," *Electr. Power Syst. Res.*, Vol. 79, No. 5, pp.796–802, May 2009.

[15] Malesani, L., Rossetto, L., Spiazzi, G., and Zuccato, A., "An AC power supply with sliding-mode control," *IEEE Ind. Appl. Mag.*, Vol. 2, No. 5, pp. 32–38, September 1996.

[16] Ramos, R., Biel, D., Fossas, E., and Guinjoan, F., "A fixed-frequency quasi-sliding control algorithm: Application to power inverters design by means of FPGA implementation," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 344–355, January 2003.

[17] Slotine, J.-J. E., and Li, W., *Applied Nonlinear Control*. Englewood Cliffs, NJ: Prentice-Hall, 1991.

[18] Wai, R. J., and Wang, W. H., "Grid-connected photovoltaic generation system," *IEEE Trans. Circuits Syst. I, Reg. Pap.*, Vol. 55, No. 3, pp. 953–964, April 2008.

[19] Tan, S. C., Lai, Y. M., and Tse, C. K., "Indirect sliding mode control of power converters via double integral sliding surface," *IEEE Trans. Power Electron.*, Vol. 23, No. 2, pp. 600–611, March 2008.

[20] Carpita, M., and Marchesoni, M., "Experimental study of a power conditioning system using sliding mode control," *IEEE Trans. Power Electron.*, Vol. 11, No. 5, pp. 731–742, September 1996.

[21] Chiang, S. J., Tai, T. L., and Lee, T. S., "Variable structure control of UPS inverters," *Proc. Inst. Electr. Eng.—Electr. Power Appl.*, Vol. 145, No. 6, pp. 559–567, November 1998.

[22] Kukrer, O., Komurcugil, H., and Doganalp, A., "A three-level hysteresis function approach to the sliding-mode control of single-phase UPS inverters," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 9, pp. 3477–3486, September 2009.

[23] Komurcugil, H., "Rotating sliding line based sliding mode control for single-phase UPS inverters," *IEEE Trans. Ind. Electron.*, Vol. 59, No. 10, pp. 3719–3726, October 2012.

[24] Gudey, S. K., and Gupta, R., "Sliding-mode control in voltage source inverter-based higher-order circuits," *Int. J. Electron.*, Vol. 102, No. 4, pp. 668–689, April 2015.

[25] Komurcugil, H. "A new sliding mode control for single-phase UPS inverters based on rotating sliding surface," *IEEE International Symposium on Industrial Electronics (ISIE)*, pp. 579–584, Italy, 2010.

[26] Holmes, D., Lipo, T., McGrath, B., and Kong, W., "Optimized design of stationary frame three phase AC current regulators," *IEEE Trans. Power Electron.*, Vol. 24, No. 11, pp. 2417–2426, November 2009.

[27] Hao, X., Yang, X., Liu, T., Huang, L., and Chen, W., "A sliding-mode controller with multiresonant sliding surface for

single-phase grid-connected VSI with an LCL filter," *IEEE Trans. Power Electron.*, Vol. 28, No. 5, pp. 2259–2268, May 2013.

[28] Zargari, N. R., Ziogas, P. D., and Joos, G., "A two switch high performance current regulated DC/AC converter module," *IEEE Trans. Ind. Appl.*, Vol. 31, No. 3, pp. 583–589, May 1995.

[29] Aamir, M., Kalwar, K. A., and Mekhilef, S., "Review: Uninterruptible Power Supply (UPS) system," *Renew. Sustain. Energy Rev.*, Vol. 58, pp. 1395–1410, May 2016.

[30] T. Bunyamin, "A high-performance SPWM controller for three-phase UPS systems operating under highly nonlinear loads," *IEEE Trans. Power Electronics*, Vol. 28, No. 8, pp. 3689–3701, August 2013

[31] Abrishamifar, A., Ahmad, A. A., and Mohamadian, M., "Fixed switching frequency sliding mode control for single-phase unipolar inverters," *IEEE Trans. Power Electron.*, Vol. 27, No. 5, pp. 2507–2514, May 2012.

BIOGRAPHIES

Muhammad Aamir received the B.E. (Hons.) degree in electrical engineering from the University of Engineering and Technology (UET), Peshawar, Pakistan, in 2007, and the Master's degree in electrical engineering from Hanyang University, Seoul, South Korea, in 2011. He is currently working toward the Ph.D. degree in electrical engineering from Power Electronics and Renewable Energy Research Laboratory (PEARL), University of Malaya, Kuala Lumpur, Malaysia. His research interests include UPSs, power conversion, and control of power converters.

Kafeel Ahmed Kalwar received the B.E. degree in electrical engineering from Mehran University of Engineering and Technology, Jamshoro, Pakistan, in 2010, and the Master's degree in electrical engineering from the University of Malaya, Kuala Lumpur, Malaysia, in 2016. Currently, he is a Faculty Member at Mehran University of Engineering and Technology. His research interests are in field of wireless power transfer system, magnetic field analysis, and high-frequency inverters.

Saad Mekhilef received the B.E. degree in electrical engineering from the University of Setif, Setif, Algeria, in 1995, and the Master's degree in engineering science and Ph.D. degree in electrical engineering from the University of Malaya, Kuala Lumpur, Malaysia, in 1998 and 2003, respectively. He is currently a Professor and the Director of the Power Electronics and Renewable Energy Research Laboratory (PEARL), Department of Electrical Engineering, University of Malaya. He is the author or co-author of more than 300 publications in international journals and proceedings. His research interests include power conversion techniques, control of power converters, renewable energy, and energy efficiency.