Simulation of 8-bit Microprocessor
(Arithmetic Logic Unit)

Developed By
Shehla Noor
(992CS118)

Supervised by
Mr. Jehanzeb Ahmad

Department of Computer Sciences
Bahria Institute of Management & Computer Science, Islamabad
University Of Peshawar, Peshawar

ABSTRACT

From the modest beginning in early 1984 at Gateway Design Automation, the Verilog hardware description language has become an industry standard as a result of extensive use in the design of integrated circuit chips and digital systems. Verilog came into being as a proprietary language supported by a simulation environment that was the first support mixed-level design representations comprising switches, gates, RTL, and high levels of abstractions of digital circuits.

This project is my first experience of digital designing. This is an accumulator-based microprocessor. First, the detailed architecture was designed, and then depending on that architecture Verilog coding was done. Although Memory based Microprocessors are better than Accumulator based, but as I was totally new to Digital Designs in Verilog, I preferred Accumulator based. It can support 11 instruction of ALU, 3 instructions of AGU and 3 instruction pipeline stages. All the instructions were tested and waveforms were generated.

The report discusses all the phases of project.

Author,

Shehla Noor

CONTENTS

1 Introduction 1

1.1 Introduction to HDL 2

1.2 Introduction to Microprocessors 4

1.3 Background of Microprocessors 7

2 Literature Survey 9

2.1 Books 10

2.2 Tools 11

2.2.1 Simucad's Silos Software 12

2.2.2 VeriWell 15

2.2.3 Xilinx 16

2.2.4 Aldec By Riviera™ 18

3 Proposed System 23

3.1 High-Level Architecture 24

3.1.1 ALU instructions 25

3.1.2 AGU instructions 26

3.1.3 Pipeline Stages 26

4 Implementation 28

4.1 The Basic Architecture 29

4.1.1 Instruction Format 29

4.1.2 Addressing Mode 29

4.1.3 Instruction Specifier 30

4.2 Modules 31

4.2.1 Arithmetic Logic Unit 35

4.2.2 Address Generation Unit 42

4.2.3 Controller 45

4.2.4 RAM 49

5 Testing 50

5.1 Stimulus 51

5.2 Tests & Waveforms 52

6 Explanation of Verilog Code 65

6.1 Behavioral Modeling 66

6.2 Data types 66

6.3 Legal Statements 66

6.4 Modules 67

6.5 Macros 69

7 Conclusions 70
8 Future Development 72
9 User Manual 74
10 Bibliography 77