ULP POWER AMPLIFIER USING 65nm CMOS TECHNOLOGY

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02-281192-001

A thesis submitted in fulfilment of the
requirements for the award of the degree of
Doctor of Philosophy (Electrical Engineering)

Department of Electrical Engineering

BAHRIA UNIVERSITY ISLAMABAD

JULY 2024

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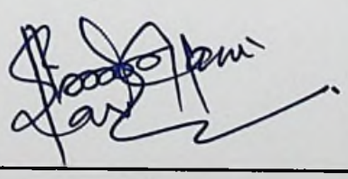
Principal Supervisor's Signature: 

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ACKNOWLEDGEMENT

I would want to express my gratitude to Engr. Dr. Najam Muhammad Amin, in the strongest terms possible, who supported this work. I was able to complete all of the publishing phases of my project because to his direction and suggestions. He has been the ideal instructor, mentor, and advisor, providing guidance and inspiration with the proper balance of knowledge and excitement. I'm happy to have worked with him and am proud of him. I learned about wireless communication and analogue IC design for the first time in the course he delivered. Many of the concepts in this thesis were created with his assistance, and it builds on the work from previous classes.

Additionally, I want to express my gratitude to Engr. Dr. Aurangzeb Rashid and Engr. Dr Mukesh Kumar Maheshwari, for their brilliant comments and suggestions, and helping me developing my ideas. Without their guidance and persistent help this dissertation would not have been possible. To me, both of them are motivating teachers who paved the way for me while I was writing my thesis. I admire all the friends and co-workers that supported me in starting the project, sticking with it, and successfully delivering it. Particularly, Engr. Dr. Razia Zia made a lot of beneficial remarks and recommendations. She helped me to get the most out of my archive study.

Finally, I would want to thank all of my family members for their support and affection, especially my parents Jawed and Rana, my sister Beena, my wife Sunia, and my brothers Asad & Ghayas, for their ongoing assistance and support while I do my research and write my paper. They all kept me going, and this work would not have been possible without them.

ABSTRACT

Power amplifier (PA) is the most power-hungry component of RF transceiver, portraying design issues. These include insufficient connectivity, power distribution, bandwidth, linearity and efficiency parameters that did not match system requirements. The primary challenge in a PA design is achieving higher efficiency while maintaining linearity over a bandwidth with wide range of output power levels. The power-added efficiency (PAE) is a figure-of-merit (FoM) that indicates how well the PA transforms DC power to RF power. Designers have raised concerns about PA in the front-end of wireless radios because of the system's significant power consumption. There has been a lot of study on PA methods for optimizing PA efficiency. It is a challenging measure in the design of PAs for various low-power IEEE 802 wireless standards. The result to this study's primary concern and problem is this issue, that presents the design and optimization of two ultra-low power (ULP) PA architectures using 65-nm CMOS technology. The first part of the dissertation is ULP Doherty PA (DPA) architecture with fixed interstage capacitances. The main amplifier and the peaking amplifier have been designed and optimized with power divider & combiner models using equivalent lumped parameters. Due to 40 MHz narrowband communication (2.4 – 2.44 GHz ISM band), it offers fixed capacitances before the input-impedance stages, for a perfect impedance matching at both stages. The novel design shows 2.1mW ultra-low DC power consumption, 29.2% PAE, and 4 dBm P1-dB compression point. The post-layout simulations show an extremely high gain of 10.14 dB, very low input-insertion loss of -11.9 dB, very strong drive current capability of 547μA & 663μA for main & peaking PAs respectively. Impedance matching is acquired to achieve the desired harmonic suppression at the output of DPA design. the consequences are all in comparison to state-of-the-art PA architectures for ZigBee and similar devices under short-range and low-power IEEE 802.15.4 WPAN standards. The second part of dissertation is class-F architecture with ET supply biasing to increase efficiency of overall PA design. The ET consists of a pre-amplifier before the envelope detector (ED) in a cascaded linear model, to increase

efficiency and to reduce DC power consumption. The gate-to-drain feedback in the PA's two cascode cells, terminated as class-F, helps to improve linearity and reduce harmonic content in the input signal. The novel design meets the requirements of the IEEE 802.11ah standard for long-range low power WLAN by using a DC power consumption of 3.75mW, a PAE of 37.1%, and an operating frequency in the unlicensed 915-931 MHz band in the United States. The chip layout size is reduced to just 0.13mm^2 by the ET inductor-less supply bias design.

Keywords - power amplifier, gain, ultra-low power, internet of things, power added efficiency, class-F, envelope tracking, gain, insertion loss, 65-nm CMOS technology

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LIST OF ABBREVIATIONS

APDN	-	Adaptive Power Distribution Network
BPSK	-	Binary Phase Shift Keying
BLE	-	Bluetooth Low Energy
BW	-	Bandwidth
CMOS	-	Complementary Metal Oxide Semiconductor
DAC	-	Digital-to-Analog Converter
DE	-	Drain Efficiency
DIBL	-	Drain Induced Barrier Lowering
DPA	-	Doherty Power Amplifier
DRC	-	Design Rule Checking
DLM	-	Dynamic Load Modulation
DSM	-	Distributed System Management
DWT	-	Discrete Wavelet Transform
EER	-	Envelope Elimination and Restoration
ET	-	Envelope Tracking
FBB	-	Forward Body Biasing
FDM	-	Frequency Division Multiplexing
FOM	-	Figure of Merit
FFT	-	Fast Fourier Transform
GFSK	-	Gaussian Frequency Shift Keying
GHz	-	Giga Hertz
GUI	-	Graphical User Interface

HFM	-	High-frequency Medium
HP	-	High Power
HSPA	-	High Speed Packet Access
HTL	-	Harmonic Tuned Load
IC	-	Inversion Current
IEEE	-	Institute of Electrical and Electronics Engineers
IoT	-	Internet of Things
ISM	-	Industrial, Scientific, and Medical
LAN	-	Local Area Network
LDO	-	Linear Drop-Out
LFM	-	Low-Frequency Medium
LINC	-	Linear amplification using non-linear components
LMN	-	Load Modulation Network
LNA	-	Low Noise Amplifier
LoRa	-	Low Range
LP	-	Low Power
LPF	-	Lowpass Filter
LTE	-	Long Term Evolution
MGTR	-	Multi-gated Transistor
MOS	-	Metal Oxide Semiconductor
NB-IoT	-	Narrow-band Internet of Things
n-MOS	-	Negatively doped Metal Oxide Semiconductor
OBO	-	Output-power back-off
OEPA	-	Out-phasing class-E Power Amplifier
OFDM	-	Orthogonal Frequency Division Multiplexing
PA	-	Power Amplifier

PAE	-	Power-Added Efficiency
PAPR	-	Peak-to-Average Power Ratio
PAR	-	Peak-to-Average Ratio
PD	-	Probability Distribution
PEP	-	Peak Envelope Power
PHMET	-	Pseudomorphic High Electron Mobility
p-MOS	-	Positively doped Metal Oxide Semiconductor
PVT	-	Process Voltage Temperature
QAM	-	Quadrature Amplitude Modulation
QPSK	-	Quadrature Phase Shift Keying
RF	-	Radio Frequency
RFIC	-	Radio Frequency Integrated Circuit
RX	-	Receiver
SCDPA	-	Switched Capacitor Digital PA
SCS	-	Signal Component Separator
SDD	-	Symbolically Defined Device
SoC	-	System-on-Chip
SSB	-	Single Side Band
TF	-	Transformer
TX	-	Transmitter
ULP	-	Ultra-Low Power
UMTS	-	Universal Mobile Telecommunications System
UWB	-	Ultra-Wide Band
WCDMA	-	Wideband Code Division Multiple Access
WLAN	-	Wireless Local Area Network
WPAN	-	Wireless Personal Area Network

LIST OF SYMBOLS

η	-	Efficiency of PA / Drain Efficiency
η_{ET}	-	Instantaneous efficiency of the ET system
α	-	Input back-off (IBO) level
γ	-	Output back-off (OBO) level
α_a	-	Activity ratio
Ω	-	Unit of resistance (ohms)
Σ	-	Summation
μ_n	-	Mobility of electrons
C_{ox}	-	Oxide capacitance
f_T	-	Transit frequency
g_m	-	Transconductance
G_m	-	Transconductance of amplifier design
U_T	-	Thermal voltage defined as $U_T = {kT}/{q}$
W	-	Width of transistor channel
L	-	Length of transistor channel
${\lambda}/{4}$	-	Quarter wavelength transmission line
R_L	-	Load Resistance
V_{DD}	-	Supply voltage at drain
I_D	-	Drain current
I_{sub}	-	Subthreshold drain current
I_{sup}	-	Super threshold drain current
V_{GS}	-	Gate-to-source voltage
V_{TH}	-	Threshold voltage
P_{out}	-	Output power
Y	-	Admittance
Z	-	Impedance