ULP POWER AMPLIFIER USING 65nm CMOS TECHNOLOGY

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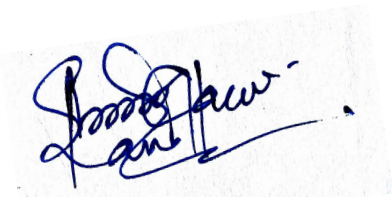

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ABSTRACT

Power amplifier (PA) is the most power-hungry component of RF transceiver, portraying design issues. These include insufficient connectivity, power distribution, bandwidth, linearity and efficiency parameters that did not match system requirements. The primary challenge in a PA design is achieving higher efficiency while maintaining linearity over a bandwidth with wide range of output power levels. The power-added efficiency (PAE) is a figure-of-merit (FoM) that indicates how well the PA transforms DC power to RF power. Designers have raised concerns about PA in the front-end of wireless radios because of the system's significant power consumption. There has been a lot of study on PA methods for optimizing PA efficiency. It is a challenging measure in the design of PAs for various low-power IEEE 802 wireless standards. The result to this study's primary concern and problem is this issue, that presents the design and optimization of two ultra-low power (ULP) PA architectures using 65-nm CMOS technology. The first part of the dissertation is ULP Doherty PA (DPA) architecture with fixed interstage capacitances. The main amplifier and the peaking amplifier have been designed and optimized with power divider & combiner models using equivalent lumped parameters. Due to 40 MHz narrowband communication (2.4 – 2.44 GHz ISM band), it offers fixed capacitances before the input-impedance stages, for a perfect impedance matching at both stages. The novel design shows 2.1mW ultra-low DC power consumption, 29.2% PAE, and 4 dBm P1-dB compression point. The post-layout simulations show an extremely high gain of 10.14 dB, very low input-insertion loss of -11.9 dB, very strong drive current capability of 547μA & 663μA for main & peaking PAs respectively. Impedance matching is acquired to achieve the desired harmonic suppression at the output of DPA design. the consequences are all in comparison to state-of-the-art PA architectures for ZigBee and similar devices under short-range and low-power IEEE 802.15.4 WPAN standards. The second part of dissertation is class-F architecture with ET supply biasing to increase efficiency of overall PA design. The ET consists of a pre-amplifier before the envelope detector (ED) in a cascaded linear model, to increase

efficiency and to reduce DC power consumption. The gate-to-drain feedback in the PA's two cascode cells, terminated as class-F, helps to improve linearity and reduce harmonic content in the input signal. The novel design meets the requirements of the IEEE 802.11ah standard for long-range low power WLAN by using a DC power consumption of 3.75mW, a PAE of 37.1%, and an operating frequency in the unlicensed 915-931 MHz band in the United States. The chip layout size is reduced to just 0.13mm^2 by the ET inductor-less supply bias design.

Keywords - power amplifier, gain, ultra-low power, internet of things, power added efficiency, class-F, envelope tracking, gain, insertion loss, 65-nm CMOS technology

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LIST OF ABBREVIATIONS

APDN	-	Adaptive Power Distribution Network
BPSK	-	Binary Phase Shift Keying
BLE	-	Bluetooth Low Energy
BW	-	Bandwidth
CMOS	-	Complementary Metal Oxide Semiconductor
DAC	-	Digital-to-Analog Converter
DE	-	Drain Efficiency
DIBL	-	Drain Induced Barrier Lowering
DPA	-	Doherty Power Amplifier
DRC	-	Design Rule Checking
DLM	-	Dynamic Load Modulation
DSM	-	Distributed System Management
DWT	-	Discrete Wavelet Transform
EER	-	Envelope Elimination and Restoration
ET	-	Envelope Tracking
FBB	-	Forward Body Biasing
FDM	-	Frequency Division Multiplexing
FOM	-	Figure of Merit
FFT	-	Fast Fourier Transform
GFSK	-	Gaussian Frequency Shift Keying
GHz	-	Giga Hertz
GUI	-	Graphical User Interface

HFM	-	High-frequency Medium
HP	-	High Power
HSPA	-	High Speed Packet Access
HTL	-	Harmonic Tuned Load
IC	-	Inversion Current
IEEE	-	Institute of Electrical and Electronics Engineers
IoT	-	Internet of Things
ISM	-	Industrial, Scientific, and Medical
LAN	-	Local Area Network
LDO	-	Linear Drop-Out
LFM	-	Low-Frequency Medium
LINC	-	Linear amplification using non-linear components
LMN	-	Load Modulation Network
LNA	-	Low Noise Amplifier
LoRa	-	Low Range
LP	-	Low Power
LPF	-	Lowpass Filter
LTE	-	Long Term Evolution
MGTR	-	Multi-gated Transistor
MOS	-	Metal Oxide Semiconductor
NB-IoT	-	Narrow-band Internet of Things
n-MOS	-	Negatively doped Metal Oxide Semiconductor
OBO	-	Output-power back-off
OEPA	-	Out-phasing class-E Power Amplifier
OFDM	-	Orthogonal Frequency Division Multiplexing
PA	-	Power Amplifier

PAE	-	Power-Added Efficiency
PAPR	-	Peak-to-Average Power Ratio
PAR	-	Peak-to-Average Ratio
PD	-	Probability Distribution
PEP	-	Peak Envelope Power
PHMET	-	Pseudomorphic High Electron Mobility
p-MOS	-	Positively doped Metal Oxide Semiconductor
PVT	-	Process Voltage Temperature
QAM	-	Quadrature Amplitude Modulation
QPSK	-	Quadrature Phase Shift Keying
RF	-	Radio Frequency
RFIC	-	Radio Frequency Integrated Circuit
RX	-	Receiver
SCDPA	-	Switched Capacitor Digital PA
SCS	-	Signal Component Separator
SDD	-	Symbolically Defined Device
SoC	-	System-on-Chip
SSB	-	Single Side Band
TF	-	Transformer
TX	-	Transmitter
ULP	-	Ultra-Low Power
UMTS	-	Universal Mobile Telecommunications System
UWB	-	Ultra-Wide Band
WCDMA	-	Wideband Code Division Multiple Access
WLAN	-	Wireless Local Area Network
WPAN	-	Wireless Personal Area Network

LIST OF SYMBOLS

η	-	Efficiency of PA / Drain Efficiency
η_{ET}	-	Instantaneous efficiency of the ET system
α	-	Input back-off (IBO) level
γ	-	Output back-off (OBO) level
α_a	-	Activity ratio
Ω	-	Unit of resistance (ohms)
Σ	-	Summation
μ_n	-	Mobility of electrons
C_{ox}	-	Oxide capacitance
f_T	-	Transit frequency
g_m	-	Transconductance
G_m	-	Transconductance of amplifier design
U_T	-	Thermal voltage defined as $U_T = {kT}/{q}$
W	-	Width of transistor channel
L	-	Length of transistor channel
${\lambda}/{4}$	-	Quarter wavelength transmission line
R_L	-	Load Resistance
V_{DD}	-	Supply voltage at drain
I_D	-	Drain current
I_{sub}	-	Subthreshold drain current
I_{sup}	-	Super threshold drain current
V_{GS}	-	Gate-to-source voltage
V_{TH}	-	Threshold voltage
P_{out}	-	Output power
Y	-	Admittance
Z	-	Impedance

CHAPTER 1

INTRODUCTION

1.1 Overview

This chapter offers the summary and historical background of this study. It first discusses the motivations behind high efficiency linear power amplification for wireless personal and local area network applications. The problem definition and contributions to improve power amplifier (PA) efficiency in CMOS ultra-low power operations are followed. Thus, concludes off by outlining the aims and organization of the dissertation.

1.2 Background

In the present world, where people use more healthcare, smart workplace, and smart home, web, social media and utility applications, everyone demands lesser time to recharge their portable devices [1]. Wireless technologies that are low-cost, power-efficient, linear, and have a small form-factor are in high demand since the last decade. These days, having a battery that has a long-life expectancy is a critical and an essential need. In addition, the challenge in current wireless communication systems is to provide high data rates in advanced modulated RF signals with a narrow-band and an ultra-low power (ULP) utilization. As a consequence, extensive research on PA design is still being conducted in both academia and industry, leading to several advancements in methods for maintaining efficiency dominating low power. The PA design has advanced significantly during the last decade, relying on very complicated transmitter topologies to address linearity and efficiency trade-offs [2].

The RF PA is widely recognized among as the most “power-hungry” component of the RF transmitter [3] and is the most challenging and important element of an RF transceiver chip [4]. In order to reduce power consumption, highly efficient RF PA is

required in portable wireless devices including laptops, PDAs, and cellular phones. These operate with the highest level of efficiency in switching (class-D, E and F) or compression (class-A, AB, and B) modes [5-7]. Efficiency and linearity must either be trade off when building and designing a power amplifier [8]. The problem arises while attempting to attain both linearity and efficiency at once, while keeping a low power consumption. Distortion levels are often backed-off until they are within acceptable levels when a randomly enveloped signal is linearly amplified through a linear class-A or class-AB PA output. Evidently, this has a considerable impact on efficiency, particularly for signals having a high or large peak-to-average power ratio (PAPR). As a result, there seems to be an efficiency versus linearity trade-off in PA design. Traditionally, when the PAPR rises, the PA must run in an output back-off (OBO) state to fulfil linearity requirements, leading in a substantial reduction in the PA's efficiency. PA contributes afterward for the majority of power usage and this efficiency reduction results in more power being dissipated. In earlier studies, a variety of PA topologies were suggested. Prior reports described linear PAs with two operating modes. First is low-power mode, while the second is high-power mode and these two operating modes are distinguished with each other with the ratio of 1:3 due to the use of load-modulation. It shows that low power mode is preferred three times more over high-power mode which as a result enhances the power back-off efficiency [9].

Increasing PA efficiency while retaining linearity and achieving all other design requirements has been an issue with no unique solution. This issue has been widely explored over many years. Various PA architectures have been proposed using classes of PA. “Pre-distortion [10, 11], out-phasing/linear amplification using non-linear components (LINC) [12], gate-dynamic biasing [13], feedback [14, 15], feed-forward [16, 17], Doherty power amplifier (DPA) [18-20], Envelope Elimination and Restoration (EER) [21-23], Envelope Tracking (ET)” [24-28], are one of the significant methods to address this issue. This research focuses on DPA and ET supply biasing techniques, specifically for short range, low power WPAN and long-range, low-power WLAN systems. A designer will find it relatively simple to realize the calculations since these are presented in a relatively easier way. One of the most widely popular methods for improving an amplifier's linearity is pre-distortion. Similarly, ET and DPA are both techniques used to improve the power efficiency of the PA. However, each has its own advantages and disadvantages, and the

choice between the two depends on the specific requirements of the application. One advantage of ET PA over DPA is that ET PA provides higher power efficiency compare to DPA, particularly at lower output power levels. This is because ET PA tracks the envelope of the input signal, which results in lower power dissipation in the PA and improved power efficiency. Another advantage of ET PA is that it is less complex to design and implement compared to DPA. This is because ET PA have a simpler power supply system compared to DPA, which have two separate power supplies for the high-power and low-power MOS transistors. On the other hand, DPAs have the advantage of being able to operate over a wider frequency range compared to ET PAs. This is because DPAs use two separate amplifiers, one optimized for high-power signals and the other optimized for low-power signals, which enables them to achieve high efficiency over a wide range of frequencies. In conclusion, all PA techniques have their own advantages and disadvantages. The choice between these depends on the specific requirements of the application, such as the required power efficiency, frequency range, DC power consumption and cost constraints.

Apart from classes of PAs, there are several techniques available from earlier studies that used bipolar devices to build similar lumped parameters, but CMOS designs are still favoured since they are more cheaper and affordable than bipolar transistors [29-31]. Today, the most significant factor in the wireless communication field is efficiency. It encompasses both spectral and power efficiency. The spectral efficiency quantifies the amount of data that can be send and received in a given amount of time. The amount of energy used to transmit power is referred to as power efficiency. Figure 1.1 graphically interprets the theory behind power efficiency by defining the concept of transmitted power over dissipated power. The power dissipated is at load, obviously, which exhibit or revel in form of heat. Particularly, a linear PA using OFDM and a constant voltage supplied yields a 20% efficiency [32].

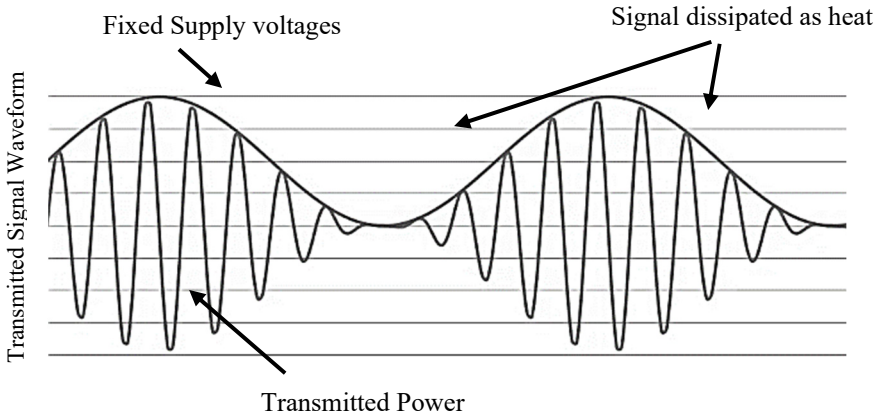


Figure 1.1: Interpretation of Transmitted Power over Dissipated Power for RF PA [32]

1.3 Research Motivation

IoT driven devices are predicted to reach a market worth of more than $75 billion in 2025, up from a market of over $15 billion in 2015. Over the ensuing ten years, this number is expected to increase rapidly. Figure 1.2 estimates a huge number of IoT-connected devices worldwide (in billions) from 2015 to 2025 [33]. As the IoT becomes a reality, the rate of change in the semiconductor market will accelerate significantly. Currently, a tremendous volume of data is sent across short and long distances using mobile communication networks like in Bluetooth connections, wireless LAN, cell phone internet protocols, and interactive media offerings including video games, movie streaming, music downloads, and cloud services. These communication systems need massive data rates and sufficient power to be handled. In order to handle this enormous growth and boost bandwidth efficiency, more complex modulated signals like OFDM, QAM, and QPSK have been used at present, and probably in future generations of wireless systems. Despite having a huge data rate and a high bandwidth efficiency, the mentioned modulation schemes' output signals have a non-uniform time-domain envelope and a high PAPR, often up to 10 dB. Traditionally, when the PAPR rises, the PA must run in an OBO state to fulfil linearity requirements, leading in a substantial reduction in the PA's efficiency. PA

contributes afterward for the majority of power usage; this efficiency reduction results in more power being dissipated.

Designing a high-efficient PA while maintaining linearity over a bandwidth and wide range of operating power levels have been a critical challenge for RF circuit designers. As a consequence, extensive research on PA design is still being conducted in both academia and industry, leading to several advancements in methods for maintaining efficiency over OBO, such as the DPA [18-20], the ET PA [24-28], and the out-phasing PA [12].

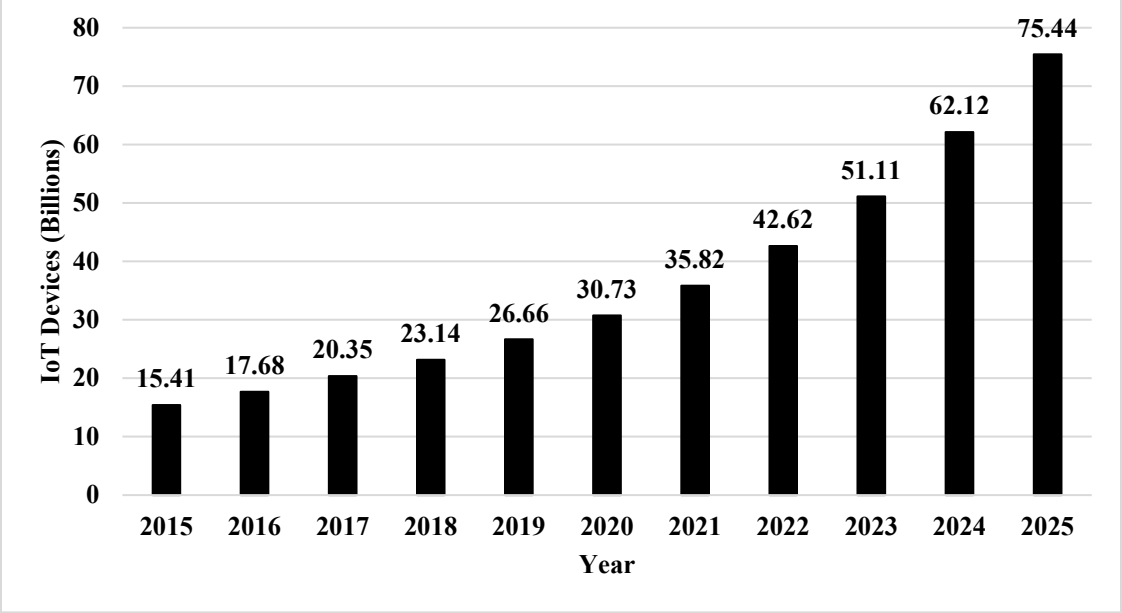


Figure 1.2: Expected IoT-connected devices worldwide (in billions) by 2025 [33]

A wireless transmitter's last building-block is an RF PA. Its job is to properly and effectively amplify the RF(Input) signal by giving power gain to the load with minimal distortion, and utilizing optimal DC power. For a prolonged battery life, ultra-low power amplifiers (ULP-PA) need serious energy constraints. With its extremely low energy usage, operating in subthreshold, gives an option for applications with such energy restrictions. Subthreshold circuits are an effective way to create systems with such energy restrictions in low to medium frequency clock ranges for wireless local area networks or

mobile applications [34-38]. Low power subthreshold models have somewhat different architecture, device circuitry, and system requirements than traditional CMOS design circuit topologies. That different architecture mainly differs from traditional architecture due to lower voltages at the biasing or the supply levels. In addition, the specifications for mixed-signal, digital, and analogue applications would vary [39, 40]. Emerging power amplifiers that need extremely low energy operation may benefit from subthreshold operation. Due to the relatively low voltage supplied, this technology is limited in its ability to sustain extremely high speeds of operation. Further, due to the lack of development in ULP technology, the subthreshold design has only been used in specialized industries despite its excellent energy efficiency. Size, weight, and cost may be just as essential as performance depending on the application. The range of power control in traditional WLAN applications like 802.11a/b/g (preferable for wide area networks) are extremely minimal or non-existent, while future WLAN systems like 802.11ah/ag are projected to include more sophisticated power management schemes to increase signal power and efficiency.

OFDM is preferred over other technologies due to its improved bandwidth efficiency [41]. One of the most important factors is power efficiency that influences PA's performance and the increase in power efficiency results in reduction of DC power consumption. Class-F PA has been quite popular in past several years, thanks to its better efficiency and low power consumption [42]. Hence all the aforementioned factors motivate to conduct research that measures the current state-of-the-art PA performance using the well-known parameters i.e., DC power consumption, linearity, power gain, power losses and harmonic rejection. Many alternative measurements exist as well, such as energy efficiency, which aims to integrate lower power consumption by measuring the energy needed to transfer a highly efficient signal at the PA output load. All of these factors contributed to the need for this research.

1.4 The Theoretical Research Gap in Designing ULP CMOS RF PA

Ultra-low power (ULP) CMOS RF PAs have become an active area of research due to their potential applications in wireless sensor networks, internet of things (IoT), and

biomedical implants. However, despite extensive research in this area, several research gaps still exist. One of the primary research gaps in ULP CMOS RF PAs achieving high efficiency while maintaining high linearity. PAs typically have a trade-off between efficiency and linearity, and this trade-off becomes even more challenging at low power levels. Achieving high efficiency while maintaining high linearity is critical for energy-efficient communication systems [43].

Another research gap is achieving a narrowband operation at low power levels. As the operating frequency of the amplifier increases, it becomes increasingly difficult to achieve high efficiency and linearity, making it challenging to achieve a narrowband operation. Moreover, the impact of process variations and device aging on the performance of ULP CMOS RF PAs is still a research challenge. As the gate biasing voltage decreases to reduce power consumption, the impact of process variations and aging becomes more significant, leading to a degradation in performance [44].

Additionally, the use of mixed-signal techniques for improving the efficiency and linearity of ULP CMOS RF PAs is an emerging research area. The integration of digital signal processing techniques in RF PAs can help achieve high-efficiency levels, while mixed-signal approaches can help mitigate the impact of non-linearities on the amplifier's performance. Overall, the research gaps in ULP CMOS RF PAs are multi-faceted and require a comprehensive approach to address them [44].

1.5 The Contextual Research Gap with Methodological Analysis in Designing ULP CMOS RF PA

To define the contextual research gap of CMOS PA, researchers have focused on specific research questions or problems related to CMOS RF PA design, such as improving the efficiency, linearity, output power, or bandwidth of the amplifier. They have also examined specific groups of participants or applications for which the PA are designed, such as low-power or battery-operated devices, high-speed wireless communication systems, or biomedical applications. Additionally, researchers considered the specific challenges and limitations of CMOS technology, such as device noise, process variation, and parasitic effects, and identify areas where further research is needed to overcome these challenges and improve the performance of CMOS RF PAs. By defining the contextual

research gap of CMOS RF PA, researchers have developed research questions and hypotheses that address important gaps in knowledge and advance the field of PA design and development. Recent researches in top-tier journals have addressed various gaps to improve efficiency and linearity of low power CMOS RF PAs.

Soltani and Mirabbasi addressed the research gap in designing ULP CMOS RF PAs with high-efficiency and specific-range bandwidth. They identified that the conventional design methodology of using a low-pass matching network to provide high input impedance and to match the load impedance to the output impedance of the amplifier is not suitable for low-power applications due to its inherent loss and reduced efficiency. To address this gap, they proposed a new design methodology using high-Q passive matching networks that can achieve high-efficiency and wide bandwidth for ULP RF PAs [45].

Chen and Breiholz addressed the research gap of designing an ULP CMOS RF PA for IoT applications. They identified that the existing CMOS RF PAs designs are not suitable for IoT applications because they require high power consumption and have limited output power, bandwidth, and efficiency. To address this gap, they proposed a new design methodology that uses a switched capacitor class-D PA to achieve low power consumption and high efficiency. They also proposed a multi-objective optimization method to simultaneously optimize the output power, efficiency, and bandwidth of the amplifier [46]. Bhuiyan and Badal also identified that the conventional CMOS RF PA designs are not suitable for IoT applications because they have limited efficiency and output power. To address this gap, they proposed a new design methodology that uses a distributed active transformer to improve the power combining efficiency and achieve higher output power, efficiency, and linearity. The proposed amplifier consists of a cascode amplifier, a distributed active transformer, and an output matching network. The distributed active transformer is used to combine the output power of multiple amplifiers, and the output matching network is used to improve the output impedance matching [47]. Murad and Mohyar proposed a new design methodology for IoT devices that uses a cascode topology and a capacitive cross-coupling technique to improve the gain and efficiency, and a matching network to improve the output power. The proposed amplifier consists of a cascode amplifier, a capacitive cross-coupling network, and an output

matching network. The capacitive cross-coupling technique is used to improve the gain and efficiency by increasing the voltage gain and reducing the output impedance, while the matching network is used to improve the output power [48]. Schmickl and Faseth addressed the gap of high-power consumption and limited gain, which can limit the PA suitability for IoT applications where low power consumption and high gain are critical. They proposed a new design methodology that uses an adaptive matching network to provide impedance matching to the load, allowing for high gain and output power. The adaptive matching network utilizes a tuneable load capacitor to adjust the impedance of the output stage, which allows the amplifier to work in a wider range of frequencies and loads. In addition, they proposed a current-reused technique to improve the efficiency of the amplifier [49].

Moloudi and Jahanirad addressed the research gap of designing an ULP CMOS RF PA with tuneable output impedance. They identified that the conventional CMOS RF PA designs have limited output impedance matching capabilities, resulting in poor output power, efficiency, and linearity. To address this gap, they proposed a new design methodology that uses a tuneable output impedance matching network to improve the output impedance matching and achieve higher output power, efficiency, and linearity. The proposed amplifier consists of a class-AB PA with an on-chip inductor, and a tuneable output impedance matching network that uses varactors to adjust the output impedance [50]. Horestani and Eshghi addressed the research gap of designing an ULP and high-gain CMOS RF PA for wearable medical devices. They identified that the conventional CMOS RF PA designs are not suitable for wearable medical devices because they have limited efficiency and output power, as well as poor gain, and often require large and complex external components. To address this gap, they proposed a new design methodology that uses a two-stage topology and a current-reused technique to improve the gain and efficiency, and a matching network to improve the output power. The proposed amplifier consists of a cascode first stage and a common-source second stage, a current-reused technique, and an output matching network. The current-reused technique is used to improve the efficiency by reusing the bias current of the first stage to drive the second stage, while the matching network is used to improve the output power [51].

1.6 Problem Statement

The RF PA consumes relatively high power as compare to other integral radio frequency integrated circuit (RFIC) elements because of the laws of thermodynamics. The high-power usage is due to the fact that a PA must offer perfect narrowband matching, high output power, linearity and power efficiency; all at the same time, which demands appropriate voltage supplied and high-power consumption. The design of a ULP PA has become a challenging research problem due to these associated specifications. One of the challenges for circuit designers is to sustain linear characteristics while assuring adequate DC power consumption with acceptable PAE. In the last two decades, the integration of RF PA on the same silicon has manufactured incredibly efficient wireless systems-on-a-chip in response to the need for portable wireless devices with, low power consumption, cheaper costs, and small form factors.

RF PA cannot achieve 100% efficiency due to the factors including resistive losses, power gain and dissipation trade-offs, non-linearities and thermal losses. There are currently far too many challenges standing in the way of converting DC power into RF power, including signal transmission losses, operating frequencies, device characteristics, and others, for anything that generates RF power to claim near-ideal performance. In certain applications, high output power and high-power efficiency are necessary PA requirements. As a result of fundamental limitations, fulfilling such criteria with CMOS technology is very challenging. Furthermore, due to the high production costs associated with conventional semiconductor technologies, interest in CMOS technology as an option for RF PA is developing. Customers' expectations have encouraged further studies to investigate completely integrated, linear, highly efficient, and low power CMOS RF PAs.

An RF PA's efficiency is limited by the large PAPR of a transmitted RF signal. In many sophisticated wireless systems, the RF signal carrying information is modulated with both frequency and amplitude to improve data rates. Frequency Division Multiplexing (FDM) systems uses multiple carriers or single-side-band (SSB) signals, as well as digitally modulated systems like quadrature-amplitude-modulation (QAM), for example, have highly time-varying envelopes and so have a high PAR value. Due to the difference in voltage between the peak and average values of the output signal increases with increasing

PAR value, the PA runs at a lower efficiency. PAs can operate at moderate to considerably reduced DC voltage level, and the average carrier voltage may be lowered even lower than the voltage supplied, depending on system parameters. As a result, RF PA efficiency and linearity must be addressed throughout a several different power levels at the output [52, 53].

The high-power consumption of CMOS RF PA has become a significant research gap, as reducing it is essential to enable low power operation and extended battery life in wireless communication systems. Moreover, current PA designs often fail to meet the required specifications for key parameters such as insertion losses, gain, DC power consumption, power-added efficiency (PAE), and output power, which are critical for efficient wireless communication. Specifically, typical PAs exhibit higher insertion losses than the desired level of below -10 dB, lower gain than the target of greater than 10 dB, higher DC power consumption than the desired level of less than 10 mW, lower PAE than the desired range of 20% to 50%, and output power levels outside the required ranges for IEEE 802.15.4 and IEEE 802.11ah standards. These limitations pose a significant challenge for modern CMOS RF PA design, and addressing these issues is essential to enable high-performance, low-power wireless communication systems [47, 54].

1.7 Research Contributions and Novelty

The contributions of this research are:

- Design and optimization of 2.1mW ULP Doherty Power Amplifier with interstage capacitances using 65-nm CMOS Technology.
- Design and optimization of High-efficient Class-F ULP-PA using envelope tracking supply bias control for long-range low power WLAN IEEE 802.11ah standard using 65-nm CMOS Technology.
- Comparison of the developed methods with state-of-the-art short-range, low power WPAN IEEE 802.15.4 and long-range low power WLAN IEEE 802.11ah communication standards in terms of DC power consumption, gain, efficiency and linearity.

This research is significant because it could lead to the development of more efficient and effective power amplifiers for a variety of wireless communication applications.

- The proposed PAs can be used in a variety of wireless communication applications.
- The proposed PAs can also be used in industrial and medical applications.
- The proposed PAs achieve a high gain, a high PAE, a low IP1-dB, and a low DC power consumption.
- The proposed PAs outperform the state-of-the-art PAs in terms of DC power consumption, gain, efficiency, and linearity.

The conflicting requirement of high efficiency has been addressed with an ultra-low power consumption. The result to this problem of highly efficient ULP-PA is the focus of this research that addresses two PA designed architectures; the DPA with interstage capacitances and class-F using ET supply bias control. The rationale for using both designs is well-addressed and the measured findings are contrasted with modern state-of-the-art PA designs (using Cadence Virtuoso IC Design 616). The prime contributions of this study are summarized in following sub-sections.

1.7.1 Design and Optimization of 2.1mW ULP Doherty Power Amplifier with Interstage Capacitances Using 65-nm CMOS Technology

The ULP Doherty power amplifier (DPA) is designed and optimized for the short-range, low power ZigBee 802.15.4 WPAN standard, using 65-nm CMOS technology. The main and peaking amplifiers are designed, simulated, and optimised at pre- and post-layouts using comparative, matched, and comparable lumped parameters. In order to obtain ULP operation and increase the linearity of the overall DPA, the performance has been carried out in the RF-nMOS subthreshold weak inversion regions. The novel designed schematic shows a DC power of 2.1mW, 29.2% PAE, 2.4GHz operational band, and 4 dBm P1-dB compression point. The post-layout simulations show an extremely high gain of 10.14 dB, very low input-insertion loss of -11.9 dB, very strong drive current capability

of 547μA & 663μA for main & peaking PAs respectively, and the consequences in comparison to state-of-the-art PA architectures for Bluetooth low-energy (BLE), ZigBee and similar devices under low-power WPAN. The results are published in:

"Muhammad Ovais Akhter, & Najam Muhammad Amin, Design and Optimization of 2.1mW ULP Doherty Power Amplifier with Interstage Capacitances Using 65-nm CMOS Technology. Published in Mathematical Problems in Engineering, 2021. DOI: doi.org/10.1155/2021/3364016"

1.7.2 Design and Optimization of High-efficient Class-F ULP-PA using Envelope Tracking Supply Bias Control for Long-Range Low Power WLAN IEEE 802.11ah Standard using 65-nm CMOS Technology

The 65-nm CMOS class-F ULP PA has been designed and optimized in accordance with the long range and low power IEEE 802.11ah standard, to increase the effectiveness of class-F PA, a supply biasing technique called envelope tracking (ET) is used. The ET adaptive supply bias includes a pre-amp just before the envelope detector (ED) to increase efficiency and reduce DC power usage. The two cascode cells terminated as class-F with gate-to-drain feedback improves linearity and reduce any harmonic content in the input signal. The novel design meets the standards of the IEEE 802.11ah standard for long-range low-power WLAN with a DC power consumption of 3.75mW and a 37.1% PAE, thereby operating in the unlicensed ranging from 915 to 931 MHz. The chip layout size is reduced to just 0.13mm^2 by the ET inductor less supply bias design. The results are published in:

"Muhammad Ovais Akhter, Najam Muhammad Amin, & Razia Zia, Design and optimization of high-efficient class-F ULP-PA using envelope tracking supply bias control for long-range low power wireless local area network IEEE 802.11ah standard using 65-nm CMOS technology. Published in IET Circuits, Devices & Systems. DOI: doi.org/10.1049/cds2.12125"

1.7.3 Comparative Analysis of Design Parameters for Modern Radio Frequency Complementary Metal Oxide Semiconductor Ultra-Low Power Amplifier Architecture Trends

This work contributes a comparative analysis of crucial design parameters within contemporary power amplifier (PA) architectures across diverse CMOS nano-meter technologies. The study assesses key factors, including signal gain, linearity, output power, and output power back-off, presenting the findings through a comprehensive table and visual representations. These insights offer valuable guidance to designers in selecting the optimal CMOS PA design tailored to specific applications. The publication delves into significant RF CMOS PA integrated implementations in the conclusion, enhancing the overall understanding of advanced PA architectures. The particulars of the publication are:

"Muhammad Ovais Akhter, Comparative Analysis of Design Parameters for Modern Radio Frequency Complementary Metal Oxide Semiconductor Ultra-Low Power Amplifier Architecture Trends, Published in MDPI Engineering Proceedings. DOI: doi.org/10.3390/engproc2023046012"

In emerging low power CMOS RF power amplifier (PA) designs for wireless personal area network (WPAN) and wireless local area network (WLAN) technologies, a number of key parameters must be optimized. One important parameter is insertion loss, also known as S11, which should be kept below -10 dB to ensure efficient impedance matching and signal transmission. Another critical parameter is gain, or S21, which should be greater than 10 dB to ensure sufficient signal amplification. In addition to these parameters, DC power consumption is a key consideration, with a target of less than 10mW to ensure low power operation and extended battery life. The range of power-added efficiency (PAE) is also an important consideration, with a target range of 20% to 50% to ensure efficient power conversion and minimized heat dissipation. Output power is another key parameter, with different requirements for different standards. For IEEE 802.15.4, the output power should be in the range of -20 to 4 dBm, while for IEEE 802.11ah, it should be in the range of 20-22 dBm. Optimizing these parameters in emerging low power CMOS

RF PAs for WPAN and WLAN technologies is critical to achieve high performance, low power operation, and efficient wireless communication.

1.8 Organization of the Dissertation

The framework of the dissertation is structured into five chapters:

Chapter 2 reviews various power amplifier topologies and characterization methods found in modern literature. It begins with an exploration of IEEE low-power standards for Internet of Things devices, followed by an examination of power amplifier classes that exhibit high efficiency. Subsequently, the focus shifts to subthreshold CMOS design and biasing schemes for Ultra-Low Power Power Amplifiers (ULP-PA). The chapter concludes with a performance summary of recent trends in ULP-PA design.

Chapter 3 is the research methodology which presents the design and optimization of two proposed ULP CMOS RF PA architectures. It starts outlining ULP DPA by first designing the PA for 2.4 GHz frequency operations, employing both ideal models and models that were provided by real-world, and real-valued library sources. Under low power conditions, the lumped parameters are used to construct both the power divider and combiner models. Excellent impedance matching of 50Ω was desired, and it has been appropriately implemented. The DPA design, simulation, optimization and test results are observed using 65-nm CMOS technology using CAD tool library analogue design environment. The load-pull demonstrates any harmonic content and power contours at ULP biasing validation for Power Added Efficiency (PAE), DC power consumption, and small signal models for S11 & S21, all qualifying under IEEE 802.15 WPAN networks. The second part of methodology involves the design and optimization of ULP ET supply bias with two cascoded cells terminated as class-F PA. It starts with the discussion of requirements for ET measurement system, generation of OFDM signal power along with its efficiency measurement. The impact of OFDM harmonics has been analysed using the Fourier series. The split integration analysis of OFDM waveforms has been tested using a conventional simulation tool. As a consequence of the ideal results, this study optimized and designed a class-F ULP-PA implementing ET supply bias in 65-nm CMOS technology.

The ET supply bias successfully incorporated the cascaded linear pre-amp with ED, representing an inductor less model.

Chapter 4 analyses and compares the results for both proposed ULP PA architectures. It includes a comparison of pre and post layout ULP DPA designs with state-of-the-art PA designs for short-range and low-power IEEE 802.15.4 WPAN standards. Additionally, it compares pre and post layout simulation results for ULP ET supply bias with state-of-the-art PA designs for IEEE long-range low-power WLAN (WiFi HaLow) devices.

Chapter 5 concludes the study, highlighting contributions and suggesting avenues for future research. The rationale behind adopting both architectures is explored, and comparisons are drawn with possible operational architectures. The ULP procedures in the RF-nMOS subthreshold moderate and weak inversion regions are detailed, maintaining the overall PA design's linearity. Measurement results are summarized and compared to modern state-of-the-art PA designs. The chapter also discusses the future of artificial intelligence in CMOS RF PA design and concludes with mapping proposed designs to Sustainable Development Goals (SDGs), including SDG 7, SDG 9, SDG 12, SDG 13, and SDG 17, with justification provided at the end of the chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

This chapter provides a detail review of several measurement approaches and architectures of power amplifier (PA), in accordance with IEEE low power standards. The chapter begins with a study of various PA classes that could achieve high-efficiency near to saturation before moving on to explore architectures that accomplish similar efficiency throughout a broad dynamic-range, i.e., at the OBO. The modern state-of-the-art examples of PA architecture are presented with thorough discussion of DPA and ET architectures. The subthreshold design and biasing technology for ULP-PA are covered in the next section. The concluding element of the chapter is the statistical summary of the ULP-PA performance for specific architecture in recent research articles.

2.2 IEEE Low Power Standards for Internet of Things

The IoT provides a new dimension to information and communication technologies where networking is always available, regardless of where you are or what you are doing. WPAN and long-range low power WLAN technologies are two subgroups of the current low-power IoT based technologies. LoRa, NB-IoT, and WiFi HaLow IEEE 802.11ah are examples of low-power WLAN technologies that emphasize on long-range communications (i.e., up to one kilometre) and offer low or medium data rates (i.e., data rates ranging from a few hundred to a few megabits per second). WPAN technologies that provide a medium or short-range communication (i.e., ranging up to a few hundred kilo-bits per second) include Zig-Bee and Bluetooth Low Energy (BLE) [55, 56]. Zigbee was

created based on IEEE 802.15.4. They are only useful in a few IoT applications because to the low transmission range of WPAN and the inadequate throughput of both low-power WPAN and WLAN.

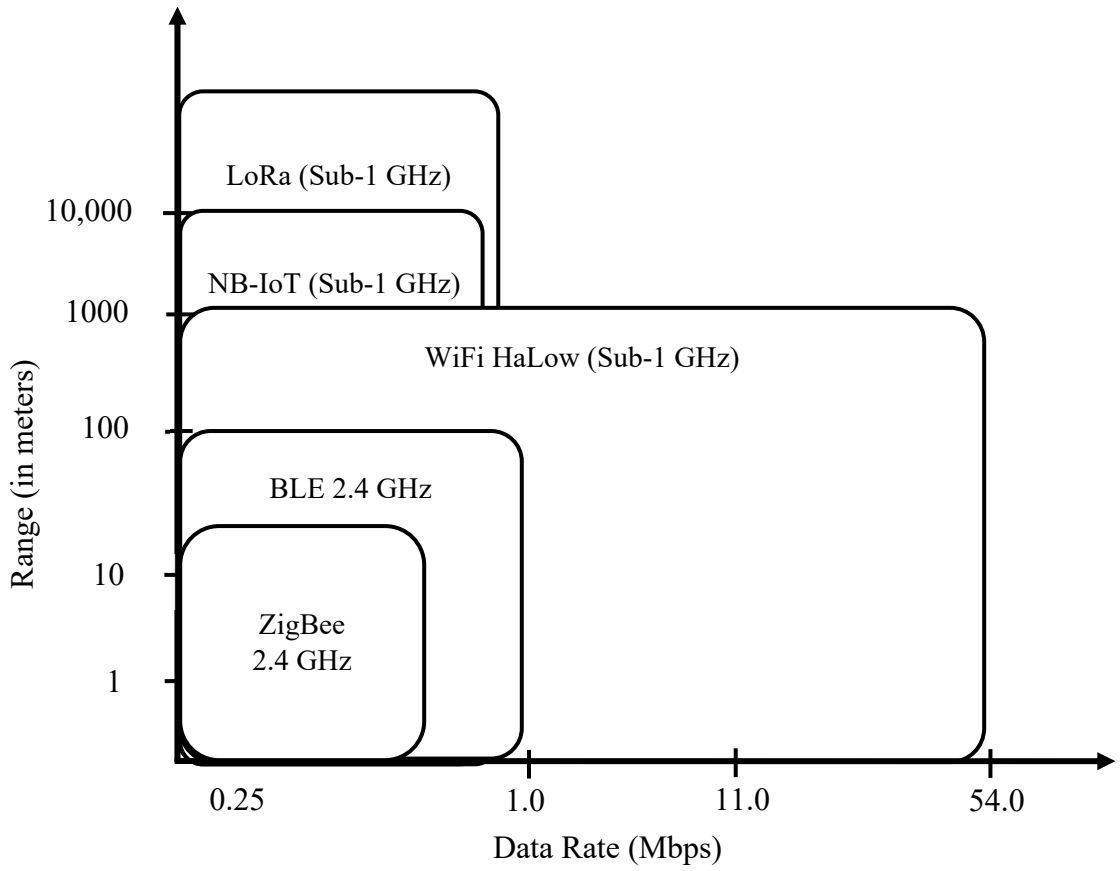


Figure 2.1: Existing IEEE Low-power Standards: The WPAN and long-range low-power WLAN technologies

There is still a need for low-power amplifiers in the field of IoT communication technology that provides enough throughput across medium transmission ranges. In order to fill this gap between WPAN and WLAN technologies, which have a maximum data rate and a medium transmission range, the most recent WiFi protocol, IEEE 802.11ah is WiFi HaLow. It was introduced as a low-power WLAN technology. The chart of wireless communication technologies, in-line to WPAN and WLAN are illustrated in Figure 2.1 [56]. Table 2.1 outlines the nomenclature of various types of Low power IEEE standards.

Table 2.1: Nomenclature of IEEE low power frequency standards [56]

Category	Technology	Operating Frequency Band	Single Channel Bandwidth (Spacing)	Modulation Technique	Range	Advantage	Disadvantage
WPAN	BLE	2.4 GHz	2 MHz	BPSK	1-100 m	Medium data rate	Short distance
	ZigBee (802.15.4)	2.4 GHz	5 MHz	BPSK	1-100 m	Medium data rate	Short distance
LP-WLAN	LoRa	Sub-1 GHz	500 kHz	Wideband linear frequency modulated chirp pulses	20 km	Long distance	Low data rate
	HaLow (802.11ah)	Sub-1 GHz	1-16 MHz	OFDM	1 km	High data rate	Medium distance
	NB-IoT	Sub-1 GHz	180 kHz	OFDM	15 km	Long distance	Low data rate

2.2.1 IEEE Short-range and Low-power WPAN Standard

IEEE 802.15.4 standard had started to fulfil the demands of WPAN devices & applications [57]. This standard is categorized into three frequency bands [58]. The first band, which operates at 868 MHz, has just one channel with a data-rate of 20 kbps and is modulated using the BPSK modulation algorithm. The second band, which operates at 915 MHz, comprises ten channels, each with a bit-rate of 40 kbps and is modulated using the BPSK modulation algorithm. The third frequency band operates at 2.4 GHz and contains 16 channels having data rate of 250 kbps apiece. The modulation strategy used 802.15 standard BPSK and QPSK. As a consequence, a Minimum Shift Keying (MSK) signal is produced. IEEE 802.15.4 has simplified linearity requirement for power amplifiers in order to make it a low-power standard by relaxing criteria for the output spectrum power mask. One can contrast the IEEE 802.15.4 standard with standard 802.15.1 Bluetooth technology. The spectrum power masks of the ZigBee and traditional Bluetooth standards are shown in Figure 2.2. This comparison demonstrates how the ZigBee IEEE 802.15.4 standard's modified linearity criteria may be used to reduce power utilization. It is based on the IEEE 802.15.4 short-range communication standard with extremely low power consumption. In the context of ZigBee PA design, linearity criteria can be used to optimize the PA's efficiency and, consequently, reduce DC power consumption. A more linear PA typically consumes more power, while a less linear PA tends to be more power-efficient (consumes less power). So, the standard 802.15.4 is more linear than traditional Zigbee [59]. The linear type PA with conduction angles less than 180^{o} (class AB, B, and C) were chosen due to the low output power delivered (around 0 dBm). The BPSK variant, which uses multi-level symbol stream which can be a binary assumption with a bit index of k [60].

There are different classes of ZigBee devices based on their output power and range. The ZigBee specification defines three classes of devices. The Class-1 devices are typically used as routers and coordinators in large ZigBee networks. Class-2 devices are used as routers and coordinators in smaller ZigBee networks. Class-3 devices are used as end devices, such as sensors or actuators, that communicate with a router or coordinator. The class of a ZigBee device also determines its power consumption and the range of its communication. Class-1 devices consume more power and have the longest range, while Class-3 devices consume less power and have the shortest range. The class of a device is

determined by the manufacturer, and the user can choose the class that best fits the requirements of their particular application. In addition to the limited bandwidth of 250 kbps, the 802.15.4 standard also includes provisions for channel access, network management, and security, which are critical components for building reliable and secure wireless networks. These features, along with the low bandwidth, make the 802.15.4 standard an excellent choice for low-power, low-cost, and low-data-rate wireless communication in IoT applications. The IEEE standard specifies the operation in the 2.4 GHz ISM band. This band is globally available and has been allocated for use by low-power, low-data-rate wireless communication devices such as ZigBee. The standard defines a number of different frequency channels within the 2.4 GHz band, each with a bandwidth of up to 5 MHz. The total bandwidth available for 802.15.4 devices is therefore around 40 MHz.

2.2.2 IEEE 802.15.4/ZigBee Power Amplifier Generalized Specifications

ZigBee PAs are specialized devices that are used to boost the power of the transmitted signal in ZigBee networks. Some of the key features of ZigBee PAs include low DC power consumption, high gain, small form factor, high efficiency, high linearity and cost effective. These PAs are designed to consume very low power, making them suitable for use in battery-powered ZigBee devices. They have high gain of +10 dB, which is a measure of the increase in power of the transmitted signal. High gain is important for extending the range of the ZigBee network. Similar to Bluetooth technology, IEEE 802.15.4 standard is divided into classes of PA as discussed earlier. The Class-1 ZigBee PAs have output power of +20 dBm (100mW) with a range of up to 100m. Class-2 ZigBee PAs have a moderate output power of up to +4 dBm (2.5mW) with a range of up to 10m. Class-3 ZigBee PAs have the lowest output power of 0 dBm (1mW) with a range of up to 1m only [61]. It is important to note that the power consumption of a ZigBee PA is closely tied to its output power, and that increasing the output power will typically result in an increase in power consumption. For this reason, ZigBee PAs are designed to be highly efficient, meaning that they convert a large proportion of the input power into output power. This helps to minimize the power consumption of the PA and extend the battery

life of the ZigBee device. In summary, the DC power consumption of ZigBee PAs is an important design consideration, as it directly affects the battery life of the ZigBee device. The power consumption of a PA can vary depending on the specific design and operating conditions, but typically it is in the range of a few milliwatts to a few tens of milliwatts [62].

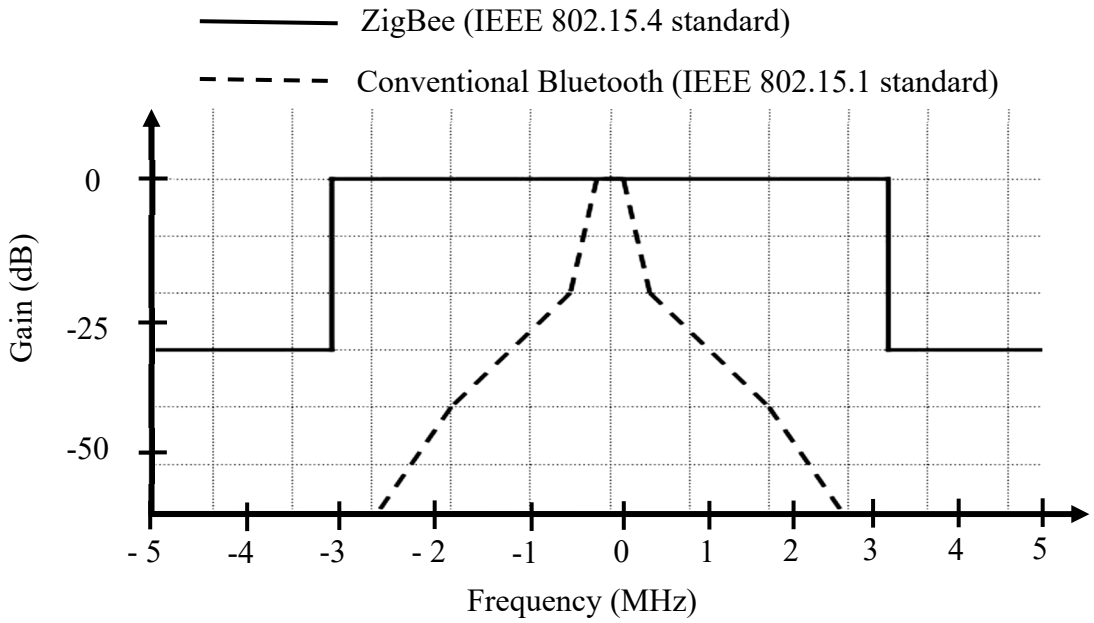


Figure 2.2: Power Spectral Mask comparison of ZigBee and Bluetooth standards [59]

2.2.3 IEEE Long Range and Low Power WLAN Standard

IEEE 802.11x standard had started to fulfil the demands of WLAN devices & long-range communication applications. One of the future ultra-low power IEEE standards is 802.11ah. WiFi HaLow is a novel technology for typical consumer, that uses reduced power to transmit data across great distances. It is still an unlicensed band under IEEE 802.11ah standard. A framework for IoT systems utilizing sub-1 GHz frequency ranges and limited bandwidth suitable for IoT equipment's is what this technology aims to deliver. The suggested forms of modulation methods include OFDM with BPSK, QPSK, and QAM, and each is dependent on the signal quality and data rate [63]. It is getting popularity

day-by-day. Additionally, it is more affordable and employs cutting-edge and dependable means of communication with other linked devices at other places [64]. Other technologies currently being used include NB-IoT and LoRA. All are considered under roof of LP-WLAN (preferred for wide area networks). WiFi HaLow is a 2017 wireless networking protocol that complies with IEEE standard 802.11ah and operates in the 915 MHz to 931 MHz frequency band (US Standards) [65]. The last phases of the IEEE 802.11ah standard's development, particularly WiFi HaLow, have been achieved, and the first chipsets that implement this breakthrough have been officially announced. Compared to 802.11g/ac IEEE standard indoor communication equipment, its range is nearly twice as large. WiFi HaLow is still in the testing phase; it doesn't currently have any large commercial buildings. The plan focuses on top-of-the-line devices with demanding execution requirements for throughput and dormancy. In order to accomplish this, 802.11ah transmits an unchangeable innovation in communication in the ISM band sub-1 GHz that relies on OFDM, offers a wide range of bandwidths (1MHz, 2MHz, 4MHz, 8MHz, and 16MHz [66]) for data transmissions, as well as freedom in modulation and coding.

2.2.4 IEEE 802.11ah/WiFi HaLow Power Amplifier Generalized Specifications

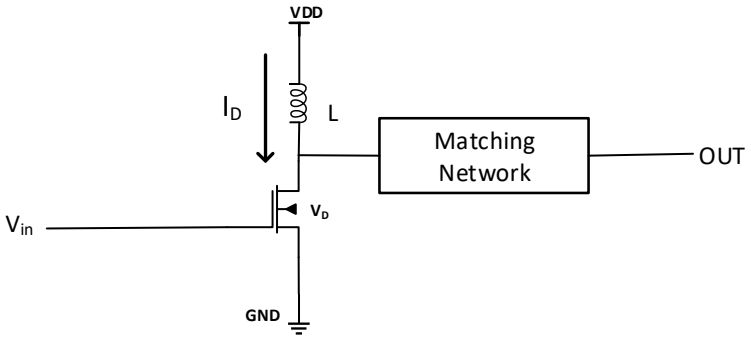
The specifications for gain, DC power consumption, range, and bandwidth of IEEE 802.11ah/WiFi HaLow can vary depending on the specific design of the amplifier and the operating conditions. The gain typically ranges from +10 dB to +30 dB. The gain of the amplifier determines the increase in power of the transmitted signal. The DC power consumption is typically in the range of a few milliwatts (ULP) to a few tens of milliwatts (LP), making it suitable for use in battery-powered devices. The range dependents on the output power and the environment, including the presence of obstacles, such as walls or furniture. The standard for range is set to a maximum of 1km as standard. With a high-gain and appropriate output power, the range can be significantly extended compared to a standard WiFi device. The bandwidth of a designed to match the bandwidth of the WiFi standard being used, such as 802.11b/g/n/ac. The standard and recommended bandwidth is either 1 MHz or 2 MHz and provide 915 MHz carriers with faster data speeds. Signals can be broadcast further away with a narrower bandwidth. Up to 26 channels may be supported

by the technology [67] with 20 dBm of output power, where the PA is capable of delivering a 14 dBm power output [66]. FFT of a 2MHz channel is 64, 56 OFDM subcarriers, 52 data-carriers, 4 pilot-tone-carriers, and a carrier spacing of 31.25 kHz (2 MHz/64) in addition to the 2 MHz channel. Each of these subcarriers may be implemented using a BPSK, QPSK, 16-QAM, 64-QAM, or 256-QAM subcarrier. There is a 1.78 MHz occupied bandwidth included in the 2 MHz total bandwidth. A guard interval of 4 or 8 microseconds is included in the 36 or 40 microsecond total symbol duration [68].

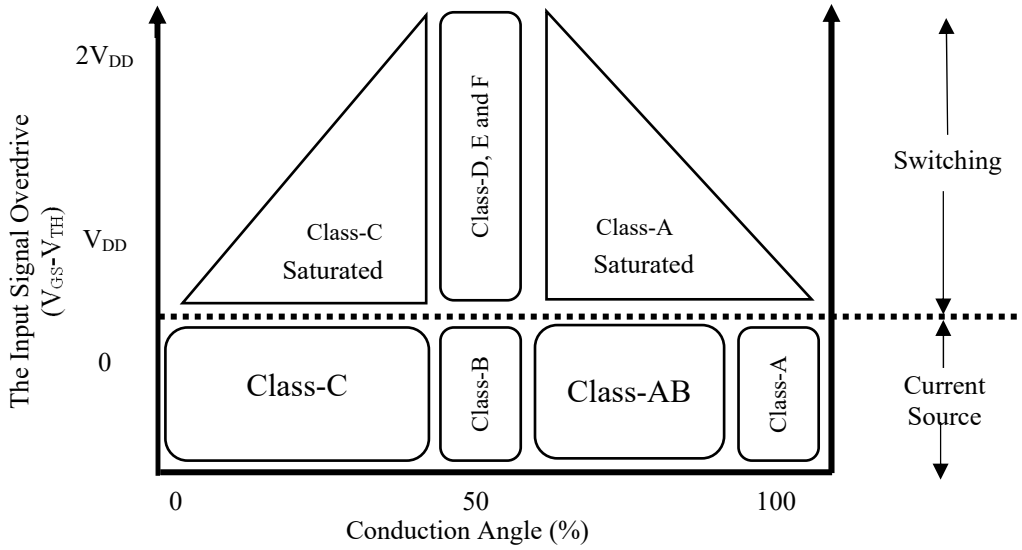
2.3 The RF PA Classification and Design Techniques

In [69] and [70], a thorough analysis of the traditional definitions of RF PA is provided. The PA may operate in class-A, AB, B, or C depending on its conduction angle, which is mostly governed by its DC gate bias, for a tiny RF input signal. Reducing the PA's conduction angle may increase efficiency (putting the device in class C operation), but at the cost of a lower output power. Increase the gate overdrive until the output transistor behaves like an on-off switch. It is an additional method to boost PA efficiency without sacrificing output power [71]. Depending on the conduction angle and load impedance, this nonlinear yet effective switched-mode operation is known as saturated class-A & C, class-E, or class-F PA. The gate overdrive of the simplified PA output stage determines the trade-off between efficiency and linearity. For a tiny RF input, the output drain voltage is a linearly amplified version of the input, supposing the output transistor is biased for class A operation. $P_{\mathrm{D}} = V_{\mathrm{D}}.I_{\mathrm{D}}$ provides the power dissipated in the output transistor. Increasing gate overdrive while decreasing power P_D will increase the PA's overall effectiveness. When the output transistor acts as an on-off switch, the output drain voltage and current are distorted square waves. The product V_D and I_D equals zero if there is no overlap between the drain current and voltage. Maximum efficiency is attained when no power is lost in the output transistor and all of the supply's energy is sent to the load. Any realizable RF PA will undoubtedly have losses as a result of the output transistor's parasitic on-resistance and the drain current and voltage's overlapping on-times. A switched-mode PA may still be quite effective, but it will also be very nonlinear. The output stage of an RF PA is illustrated in Figure 2.3(a). It is made up of an impedance matching network, an RF choke and an

output transistor. This PA's conduction angle, input signal overdrive, and output load impedance all affect its performance. Figure 2.3(b) demonstrates how the input signal drive and a conduction angle of a MOS PA correspond to its classical definitions [70]. It shows that based on a PA's conduction angle and input signal overload; it may be functioning in either of the standard operational modes.



(a) The output stage of a typical RF PA



(b) The traditional explanation of RF Pas [70]

Figure 2.3: (a) An RF PA output stage in a simplified form (b) Traditional explanations of RF PAs.

The various kinds of PAs are classified based on their electrical properties, circuit architecture, and operating mode. For example, the conduction angle is the percentage of a simulated sinusoidal wavelength that results in a device conducting during one operational cycle. PAs may be further differentiated depending on how the bias-point is chosen. The drive-level and the biasing-point together determine the conduction-angle, and dictates where the RF (input) cycle is active. Conventional PA designs are traditionally classified into four categories i.e., from class-A to class-F. Traditional transconductance amplifier technologies like as PA in classes A and B are often designed in applications needing significant amplification linearity, such as in most wireless radio equipment. The output characteristic of a class-A PA is biased at a position that allows output-current to flow through out complete cycle of the input signal. In other words, the transistor has a 360^{o} conduction angle because it is biased in the middle of the transfer characteristic's most linear region, and reasonably good linearity. Apart from that, at peak envelope power (PEP), the highest ideal efficiency that a class-A PA can achieve is 50%. Unfortunately, these methods strictly limit power efficiency, making it impossible to achieve the needed size and cost reductions. Harmonic-tuned saturation and switching amplifiers offer a higher-efficiency option in situations where distorted AM/AM and AM/PM is tolerated to some extent [72, 73]. A transistor biased as class-B induce output conduction for only half of the input cycle, resulting in a 180^{o} conduction angle. At PEP, this results in a lower power gain (3 dB) and an optimal drain efficiency of 78.5 percent for class-B (more than class-A). The ideal class-B PA is linear because the conduction angle does not vary with the applied input level. Moreover, based on the characteristic soft turn-on behaviour of a circuit, less linear than class-A is class-B, resulting in a distorted output waveform and cross-over noise. A class-AB amplifier is constructed when the bias of the transistor is between classes A and B, with a conduction angle of 180^{o} to 360^{o} and an optimal attainable efficiency of 50 to 78.5 percent.

The class-AB amplifier uses a relatively limited amount of quiescent current flow in comparison to the class-B amplifier, to bias the transistor just beyond the device's threshold level. This results in a conduction angle that is much higher than 180° but less than 360. It's worth noting that class-C amplification occurs when a transistor's operational bias-point is decreased to the point where there are conduction angles that are lower than

180°. This may result in a higher drain efficiency operating of about 90% but with low gain and linearity due to substantial distortion in the signal output. As the input and output signals have a quite linear relationship, class-A, class-AB, and class-B PAs are often referred to as linear PAs. Amplifiers in the class-E and class-F modes may attain efficiencies of more than 80%, and even proceeding to 100%, making them suitable where efficiency is a priority. Table 2.2 represents the various classes of all well-known PAs [74].

Table 2.2: Comparison of various classes of PA [74]

Mode	Class of PA	Mode of Operation	Conduction Angle (%)	Drain Efficiency (%)
Linear	A	Compression/ Current Source	100	50
	AB	Compression/ Current Source	50 – 100	50 – 78.5
	B	Compression/ Current Source	50	78.5
	C	Compression/ Current Source	<50	100
Switch	D	Switch	50	100
	E	Switch	50	100
Harmonic Tuned	F	Switch	50	100

2.4 Scope of Work for an Ultra-low Power High-Efficient CMOS RF Power Amplifier Design

Designing ultra-low power, high-efficient CMOS RF power amplifiers is an active area of research and development, with ongoing efforts to improve the efficiency, linearity,

bandwidth, and noise performance of these amplifiers. Some recent advancements and challenges in this field include:

- **High efficiency:** One of the main challenges in designing RF PAs is achieving high efficiency while maintaining good linearity and low noise. High efficiency is a critical requirement for WPAN and WLAN applications, as it enables longer battery life and improved spectral efficiency. Recent research has focused on exploring new circuit topologies, such as switch-mode PAs (Class-E, Class-F, Doherty and Out-phasing), to improve efficiency.
- **Low power consumption:** The trend towards low power consumption in portable devices has led to a growing demand for ultra-low power RF PAs. This requires careful optimization of the circuit design to minimize power consumption while still achieving high performance. WPAN and WLAN applications require low power consumption for increased battery life and reduced heat dissipation. Recent research has focused on reducing the power consumption of CMOS RF PAs by exploring techniques such as biasing and supply voltage optimization, duty cycle control, and envelope tracking.
- **Linearity:** WPAN and WLAN applications require high linearity to ensure reliable communication and to minimize interference with other devices. Recent research has focused on improving linearity of CMOS RF PA through techniques such as linearization, pre-distortion, and feedforward**.**
- **Integration with digital circuits:** With the trend towards System-on-Chip (SoC) integration, there is a need to integrate RF PAs with digital circuits on a single chip. Recent research has focused on developing techniques to integrate RF PAs with digital circuits (like digital modulator or oscillator) to minimize interference and achieve high performance in a noisy digital environment.

Overall, the recent scope of work in designing ultra-low power, high-efficient CMOS RF PAs for WPAN and WLAN applications is focused on reducing power consumption, improving efficiency, linearity, wideband operation, and integration with digital circuits. These efforts are aimed at meeting the growing demand for low power, high performance, and reliable communication in wireless networks [75-78].

2.4.1 Enhancing PA Linearization

To move the "linear" PA closer to ideal linearity is the main objective of PA linearization. Since the PA transistor handles a huge signal, when the PA gets close to the 1-dB compression limit, the transistor's transconductance will be nonlinear. A class-AB PA's AM-AM plot is shown in Figure 2.4. The transistor's AM-AM is also caused by nonlinear capacitance and nonlinear input/output impedance. The 1-dB compression threshold is moved toward the saturation point when linearization methods (such as pre-distortion, feedback, and feedforward) are used in the PA. The PA efficiency is increased by boosting the output power to 1-dB compression point [79].

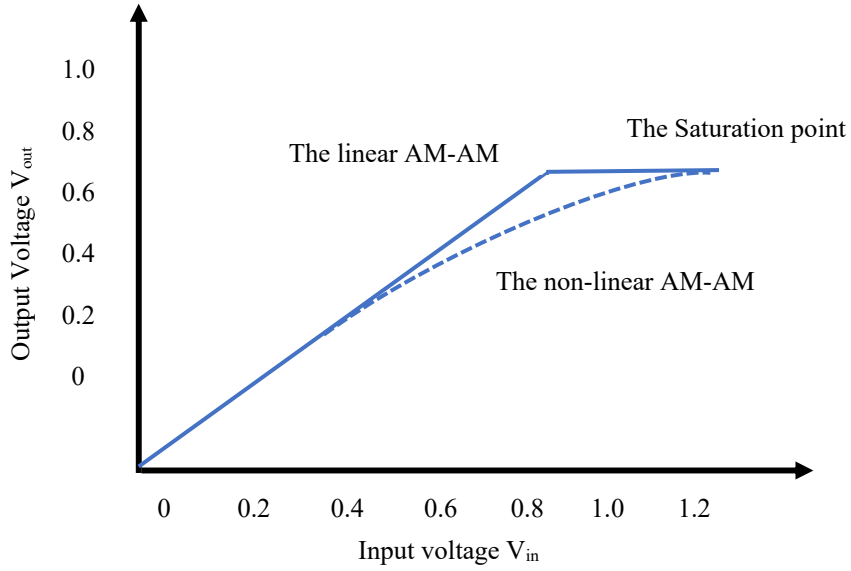


Figure 2.4: Gain compression and the impact of linearization are seen on a PA gain plot [79]

2.4.2 Enhancing PA Drain Efficiency and Power-Added Efficiency

The Drain efficiency (DE) is the measure of how well the PA delivers output power in relation to DC input power. It is defined as the proportion of the amplifier's output power to its DC input power $\left(\eta = \frac{P_{out}}{P_{DC}}\right)$. This kind of efficiency, however, might be deceptive to RF designers since it disregards how much power the amplifier consumes. A PA might

have a very low gain while yet having a good drain efficiency. The ratio of a PA's effective output power to its DC input power is known as its power added efficiency (PAE). The effective output power is determined by calculating the difference between input and output power. Effective output power is calculated as the difference of output power and the input power i.e., Pout - Pin, where Pout is the output power the PA delivers and Pin is the input power the PA can handle. This then divides the DC power supplied to the PA. It is quantified as a percentage [80].

$$PAE = \left(\frac{P_{out} - P_{in}}{P_{DC}}\right) 100 \tag{2.1}$$

DE does not take into account how much power is used by the amplifier; it might be deceptive to RF engineers. An amplifier may have a very low gain while yet having a good drain efficiency. To determine the percentage of the DC input power that amplifies an input signal, the PAE parameter is a useful tool. If a PA is 100 percent efficient, all of its input power is transformed into output power. Since there are no such PAs in reality, some DC power is lost during conversion as heat that is dissipated. Due to the extra power provided by its DC source, an amplifier has the ability to amplify an input signal. Therefore, PAE is often preferable to drain efficiency. In general, PAE is considered while developing, debugging, validating quality assurance, and testing ICs in production. Figure 2.5 shows the relation between the power gain (in dB), and the output power measured over the input power (both in dBm) [81].

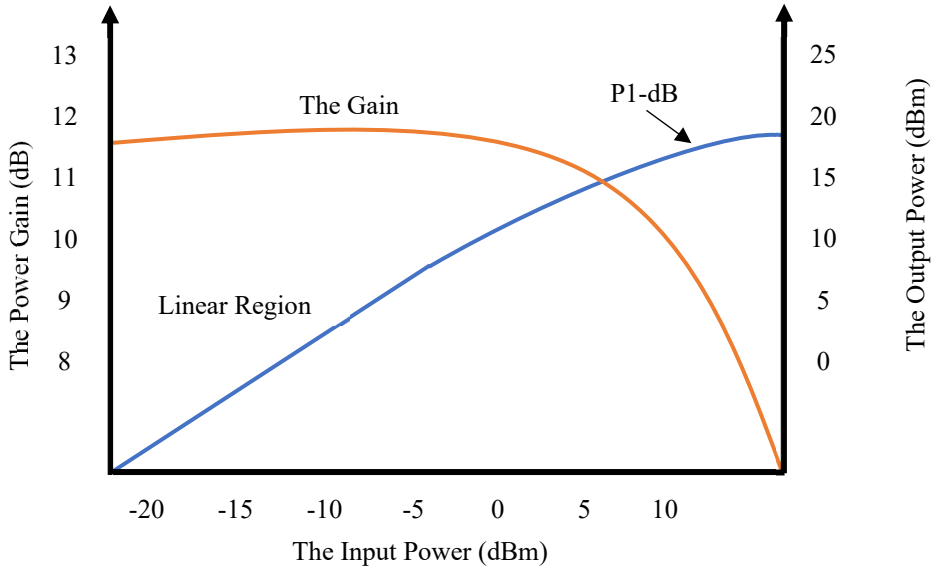


Figure 2.5: The Power Gain (dB), The Output Power (dBm) over the Input Power (dBm) [81]

2.5 Modern Trends in RF PA Design Architectures

A number of methodologies have been proposed to optimise the efficiency and output at OBO by dynamically adjusting the voltage supplied or the load-impedance. On the basis of RF PA classes, the architectures have been proposed. Figure 2.6 sub-divides the PA design to two main PA architectures i.e., the dynamic load-modulation PA and dynamic supply PA architectures. RF designers have emphasized on load-modulation as one of the potential techniques to increase PA efficiency in OBO. To obtain high efficiency, this strategy alters the load-impedance that is delivered to the PA's output. The magnitude of output power is also optimised by using aforementioned method [82]. The load modulator is appropriate for narrow-bandwidth operation and delivers high efficiency with considerable output noise. The dynamic-supply modulator PA is either a switching, linear, or a hybrid form of modulator. In contrast, the load modulator has a lower bandwidth and more noise (ripples) in the output, but it is less efficient than dynamic supply modulator [83].

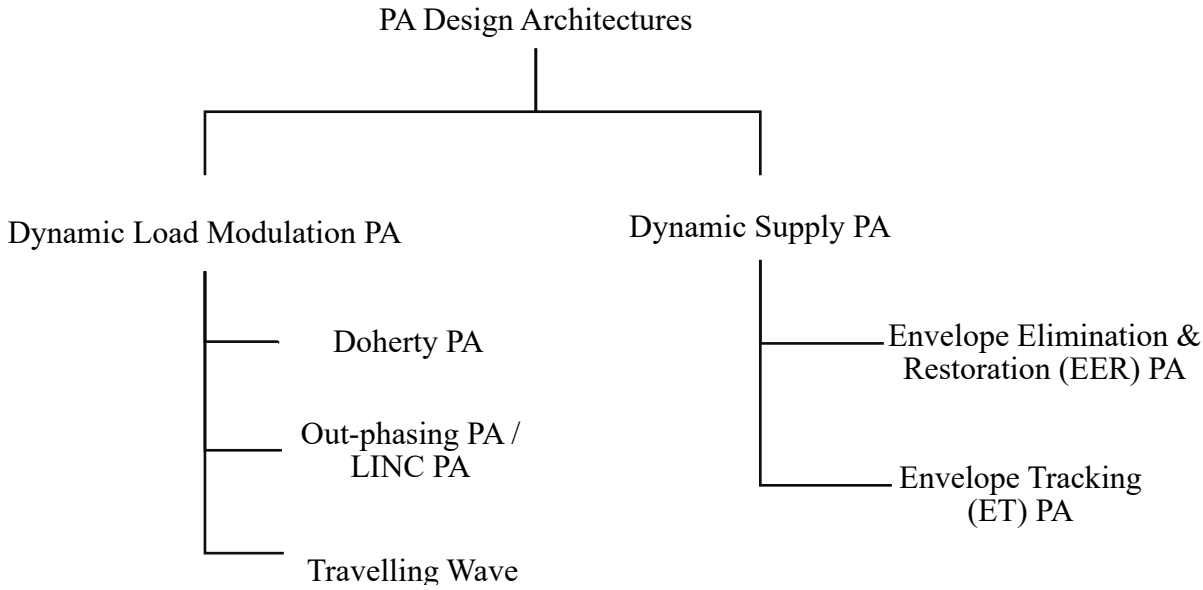


Figure 2.6: Modern Trends in PA design architectures

A summary showing the number of published articles and trends of afore-mentioned RF PA design techniques are presented in Figure 2.7. This study was carried out in [75], which concentrated on describing the globalization, cross-affiliation cooperation, research cycle, and architectural trends as well as looking at the development trend of RF PAs. The rising trends for DPA and ET PA architectures show their importance in designing a high-linear and a low-powered PA.

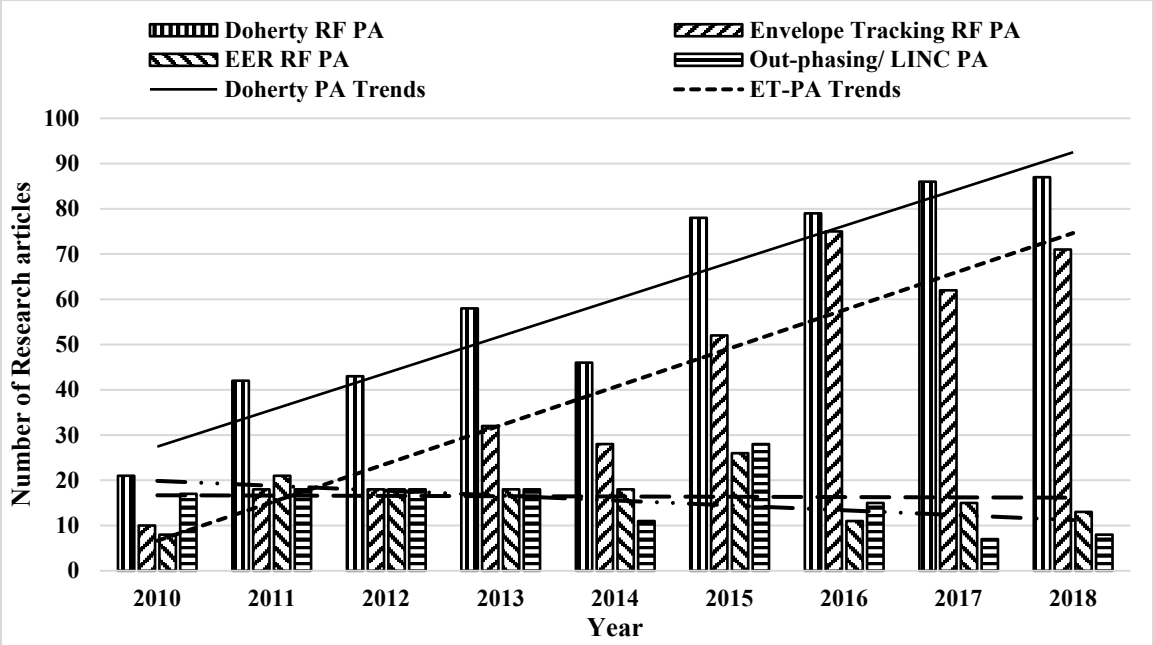


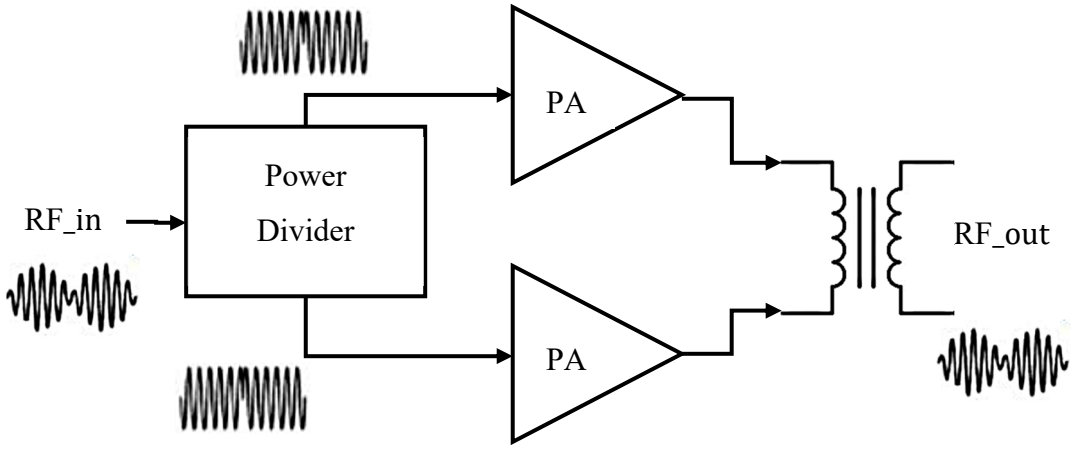
Figure 2.7: RF PA Research Trends [75]

2.6 Doherty Power Amplifier Design

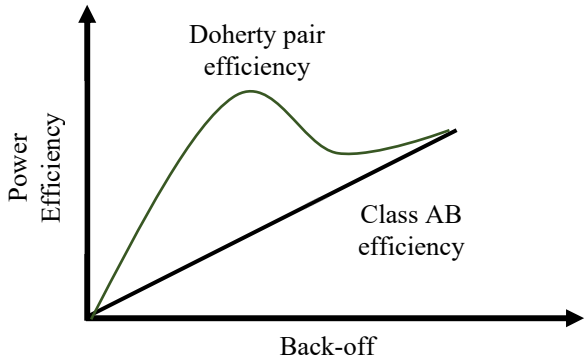
The Doherty Power Amplifier (DPA) is a multiple-device design with high efficiency that is presently used in both short and long-range wireless communication devices. W. H. Doherty developed it for the first time at "Bell Telephone Laboratories Inc." in 1936 to increase the poor efficiency of MW broadcasting transmitters that used vacuum tubes [84]. A considerable increase in average efficiency across dynamic range is shown when evaluating the total efficiency of the two devices to a comparable peripheral balanced amplifier. Thanks to the active load-modulation idea, a simple RF(Input) and RF(output) layout may achieve optimal efficiency throughout OBO in the range of 6 dB for classical DPA, and more than 6 dB for extended dynamic range DPAs.

2.6.1 The Classic DPA

The classic DPA technique is demonstrated in Figure 2.8, which in some ways is seen as a very sophisticated analogue design. The traditional DPA design relies on an unbalanced power splitter configuration at the structure's input and a static bias technique to adjust and control the peaking amplifier's conductivity, in order to make the main and peaking amplifiers at PEP operate at the same nominal current. Due of its ease of use and simplicity, the classical DPA is a popular implementation. It has a main amplifier that is constantly active and a secondary, peaking amplifier that only activates when the input signal strength exceeds a set threshold, such as 6 dB. The fundamental DPA invention is merging of the two transistor drain currents via a quarter-wave transformer, which in reality is a section of transmission line and transforms the input current at one port into an output voltage at the other port. A symmetric LC- Π network does the same thing. The main amplifier is often biased in as class-AB while the peaking amplifier is generally class-C biased. Theoretically, a change in phase between two input signals should be 90 degrees, but in practice, this number varies depending on the features of the device, such as drive dependent S_{11}, and the transmission line types used. DPA is often considered as class AB replacement only. Due to its flexibility for signals with a high PAPR and capacity to keep high efficiency at peak and average power levels, this design is typically utilized in current communication systems. Modern matching techniques have also been introduced to enhance the efficiency of DPA. Load modulation is one of the technique that describes the variations in impedances for both the main and the peaking PAs in the high and low power regions [76].



(a) Traditional DPA concept with schematic block diagram



(b) Output Back-off (OBO)

Figure 2.8: (a) The traditional DPA concept and (b) the OBO efficiency

2.6.2 Modern Techniques in DPA

Modern DPA is an architecture for load modulation, that incorporates the dynamic adjustment of load-impedance to achieve maximum efficiency. In this case, the main amplifier has been provided with the load after it has been shifted from $R_{opt}/2$ to $2R_{opt}$ (modulated), as seen in Figure 2.9. Based on load-modulation technology, DPA is one of the most extensively used transmitters for handset and base station applications.

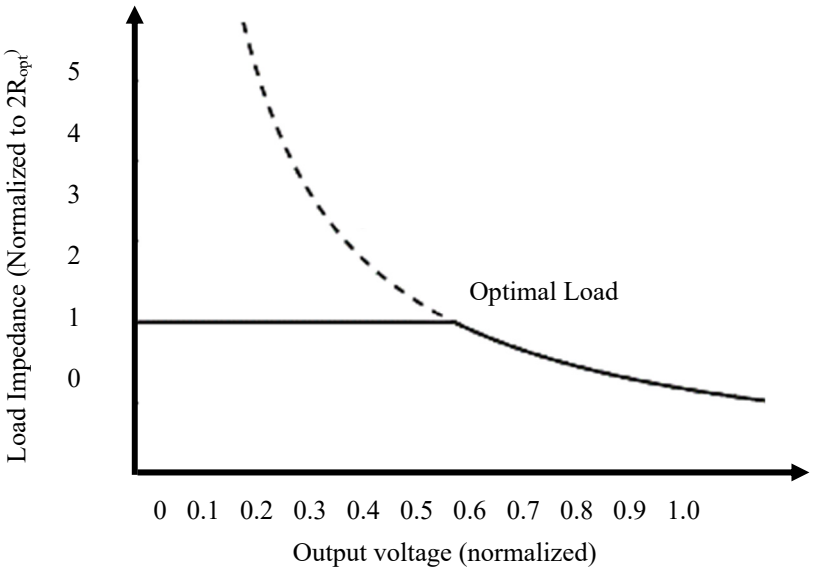
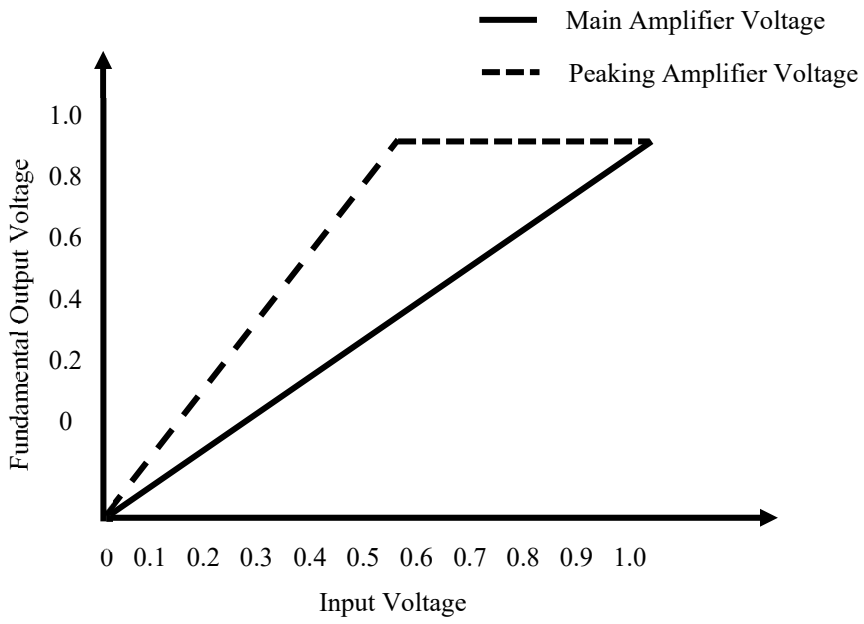
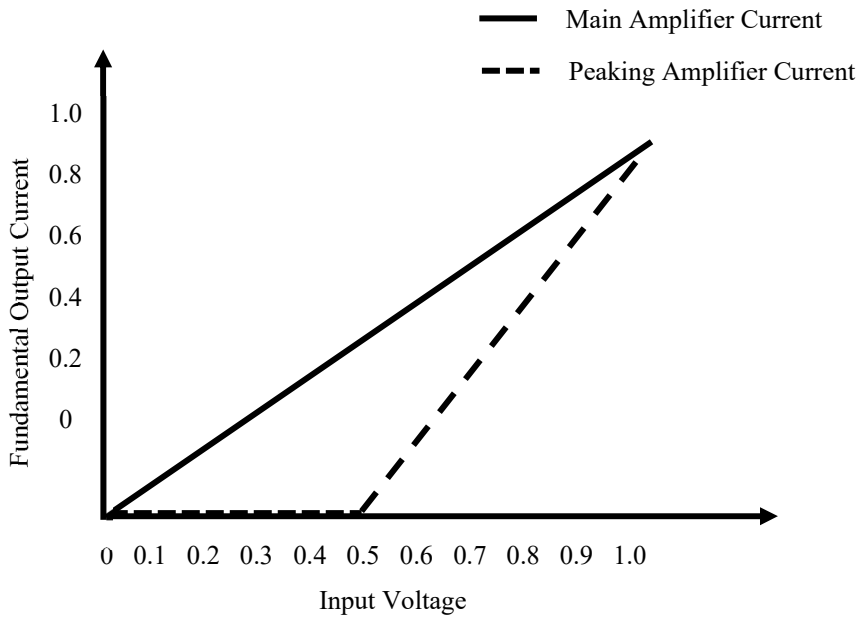


Figure 2.9: DPA optimum load-impedance for both ideal and real component design

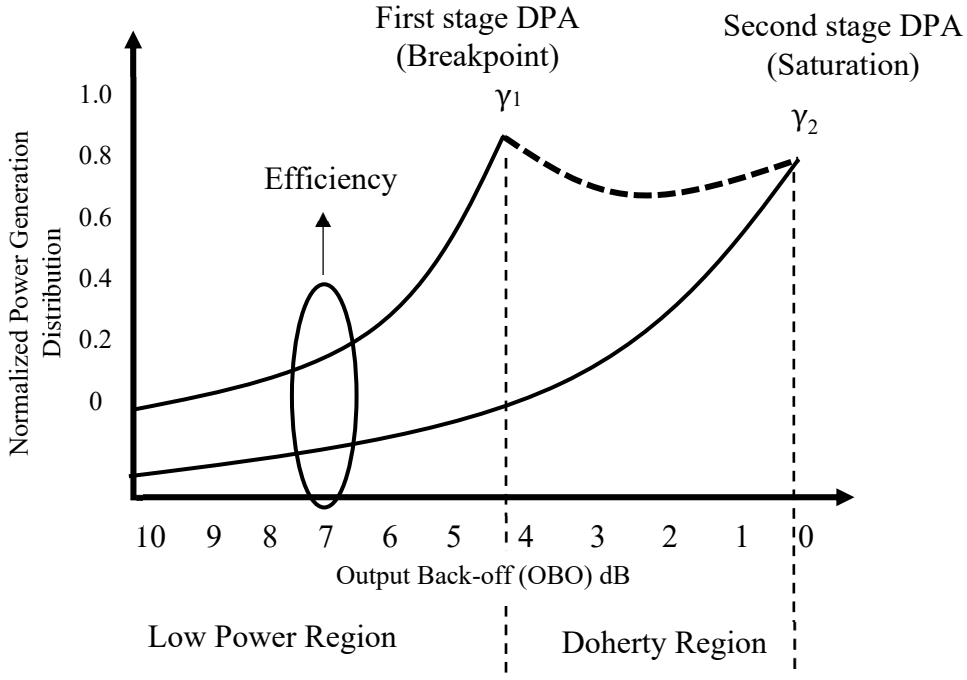
The primary output voltage amplitude of the main amplifier will rise linearly as the input drive level is maintained until it hits the transition point, which is also defined as its peak (and maximum efficiency). Keep in mind that the peaking amplifier is inactive and in the low power region. It is significant to observe that the voltage at the peaking amplifier's output has been increasing linearly up to the transition point, despite being idle. We can observe from Figures 2.10(a) and Figure 2.10(b) below that the voltage and the current behaviour up to the changeover point is likewise linear. For the case when both the devices are equal, $\alpha_1 = \alpha_2 = 1$ (where α represents the input backoff level) and $\gamma_1 = \gamma_2 = 1/2$ (where γ represents the output backoff level - γ_1 is the break-point while γ_2 represents the saturation) and these are obtained using the current, voltage and impedance profiles of designed class-B and class-C amplifier. Figure 2.10(c) expresses the peak efficiency that is reached at the OBO level γ.



(a) Fundamental normalized output voltage



(b) Fundamental normalized output current



(c) Peak efficiency

Figure 2.10: Fundamental normalized (a) output voltage and (b) output current for main and peaking amplifiers over fundamental input voltages (c) the peak efficiency that is reached at the OBO level γ.

Wideband DPA design may also be benefited by adjusting the load. Nevertheless because of the limitation brought upon by the quarter wavelength impedance transformer, DPA designs are restricted and unable to process wide bandwidths (>20%). In study [85], a unique wideband high-efficiency DPA has been presented that successfully matches the peak power and the OBO points using a "two-point matching" technique. The benefits of the suggested rectifier employing the two-point matching approach include a wide bandwidth with good efficiency at peak power and OBO points, which broadens the PA's application scope. More than 45% of the drain efficiency $\left(\frac{P_{out}}{P_{dc}}\right)$ is achieved at the 6 dB OBO. Multigated transistors (MGTRs) are used in the primary PA in [86], which is a different Doherty approach. It reduces the DPA's third-order intermodulation distortion but with more suitable approach for a low power design instead of an ultra-low power design. As a consequence, linearity is significantly improved. Yang proposes an improved and amended load-modulation network (LMN) to simultaneously improve the OBO range and the DPA bandwidth [87]. Analysis is used to determine the relationship between the recommended LMN parameters and the broadband efficiency at various OBO levels. The designed DPA has a 9 dB OBO range and works between 1.4 and 2.5 GHz.

Modern DPA implementations, in particular, focus on the many methods adopted to regulate the peaking amplifier's conduction behaviour in order to ensure equal maximum current contributions from both amplifiers at PEP. These methods are specifically Input Attenuation (IA) and Bias Adaption. The IA-DPA approach's key principle is to use applied input signal strength rather than input bias offset to adjust the equivalent conduction of the peaking and main amplifiers [88]. Conceptually, the magnitude variation may be easily accomplished by adding a variable attenuator and a symmetrical power splitter to the peaking amplifier's input signal path. The signal's relative input phase delivered to the peaking amplifier may also be adjusted to produce the desired output. Utilizing distinct and distinguished phase-coherent sources, one serving as the main amplifier and other serving as the peaking amplifier, is an alternative strategy. This fundamental concept has been developed in a number of recent studies to increase efficiency, as demonstrated in [89]. It uses a dual input power configuration for driving peaking and main amplifiers and digital

phase alignment to overcome performance degradation. Comparing this to the traditional analogue DPA, this design increased the PAE by 10%. With separate input sources connected to the input circuit of both the main and peaking amplifiers, the innovative & novel research approach reported in [90] presents an optimized design strategy for DPA design. Peaking PA fixed class-C biasing in conventional DPA results in a delayed contribution of current compared to an immediate current contribution after the transition point because of the soft turn-on behaviour of transistor device. Doherty design must deal for these issues, which eventually leads to reduced efficiency in the vicinity of the transition region. In order to get the best Doherty behaviour, the AB-DPA is one technique to increase efficiency [91-93]. It involves changing the gate voltage of the peaking amplifier in response to the input signal envelope. It might be argued that bias regulation at the modulation frequencies is easier (and less expensive) than RF amplitude regulation for IA-DPA. In [94], Zhang presented an innovative AB-DPA design in which the efficiency improvement is accomplished by giving the main-PA and peaking-PA, the ideal biases in accordance with the input power level. An adaptive power distribution network (APDN) is used to create the input matching network. As a result, reduced RF power loss at low power levels. This means that ideal load-impedances are attained at each power level while preserving a relatively small chip-size.

Conversely, compared to traditional DPA, the input attenuation's overall methodology necessitates input magnitude detection be positioned at the peaking amplifier path, which significantly raises design complexity and, subsequently, cost. The most frequently employed technology for improving the PAE is the adaptive bias strategy. This technique's impact is, however, sensitive to frequency change. In order to reduce the adaptive bias technique's frequency-related effects [95], introduced a unique technique identified as the 45 MHz to 2.5 GHz CMOS PA's common-source (CS) adaptive bias. The maximum PAE observed with the recommended PA at 500 MHz frequency is 44.61%, which is an excellent performance. The adaptive bias technique may be used to adjust the device voltage supplied in addition to adjusting gate bias. By adjusting the voltage supplied, many research investigations have been carried out to create higher efficiency. The majority of adaptive bias approaches are either restricted to bias the gate voltage of the main amplifier or use DC supply and do not correspond to varying the gate biasing voltage

of the peaking amplifier. As a result, the gate controlled adaptive bias DPA design is prioritized in this research by optimizing the main amplifier's gate voltage.

The essential component in the design and modelling of RF PA is the CMOS device. Due to the signals' high PAPR values, utilized in such systems, the average efficiency of a linear power amplifier (running in class B or AB) when used in current radio transmitters is relatively low. Thus, several methods to improve the efficiency of the amplifier at OBO from the peak value have been suggested in the literature. The efficiency of a class-B biased PA is directly proportional to the ratio of the transistor's drain voltage swing to its drain supply voltage, which gives birth to the fundamental concept of increasing back-efficiency. The output voltage swing's amplitude follows Ohm's law, or, in the case of an ideal transistor model and a load impedance, RL.

$$V_1 = I_1 . R_L \tag{2.2}$$

where R_L is the load resistance, I_1 and V_1 stand for the fundamental drain current and voltage components, respectively (at fundamental frequency). Commonly referred to as the optimal load impedance of the transistor, R_{opt}, R_L is chosen to get the best performance at peak power. In other words, $R_L = R_{opt}$ causes complete rail-to-rail voltage swing at the device's nominal peak current, which means that the maximum efficiency and peak output power are simultaneously achieved. R_{opt} for a certain device is provided by,

$$R_{opt} = \frac{(V_{DD} - V_k)^2}{2P_{out,max}} \tag{2.3}$$

Many methods developed to enhance efficiency at a specified power level have their roots in equation 2.3. These methods may be generally split into two groups. The first one maintains the load resistance RL (as observed in equation 2.2) as the ideal load impedance over the whole power range. Actually, according to equation 2.3, the transistor drain supply voltage varies as a function of Pout, i.e., proportionate to the signal envelope. These methods are referred to as drain supply modulation methods. Unfortunately, the nonzero knee voltage of the device significantly reduces the efficiency increase at high OBO. Alternately, to maintain the greatest voltage swing and efficiency throughout a

certain power range, one might vary the transistor's effective load impedance, also known as the load impedance "seen" by the transistor. The Doherty architecture is the most well-known member of the latter category, which is referred to as the load modulation approaches. In this part, the two categories of approaches will be examined.

2.7 Out-phasing / LINC PA

The out-phasing modulation method was designed to increase the linearity and efficiency of AM broadcast transmitters. Significantly later, under the term/ moniker LINC (linear amplification using nonlinear components), its use was expanded to microwave frequencies. An out-phasing transmitter, depicted in Figure 2.11, operates as a linear system by combining the outputs of two non-linear signals driving PAs with variable time-varying phases and constant amplitudes in accordance with the input signal envelope, for amplitude-modulated signals over a wide range of input signal levels and having a linear transfer function [96]. By narrowing down their impedance matching and biasing circuits, the optimum power efficiency at saturation should be delivered via PA tuning. This results in the utilization of the highly nonlinear switch-mode class, which cannot tune harmonics. While amplifiers may function very effectively, the leftover power at the combiner's output will decide the LINC system's overall efficiency [97]. Although narrowband is supported by this design, special power-combiners are needed. Specific phase-compensated dividers are needed since Wilkinson / hybrid ones do not operate sufficiently in LINC.

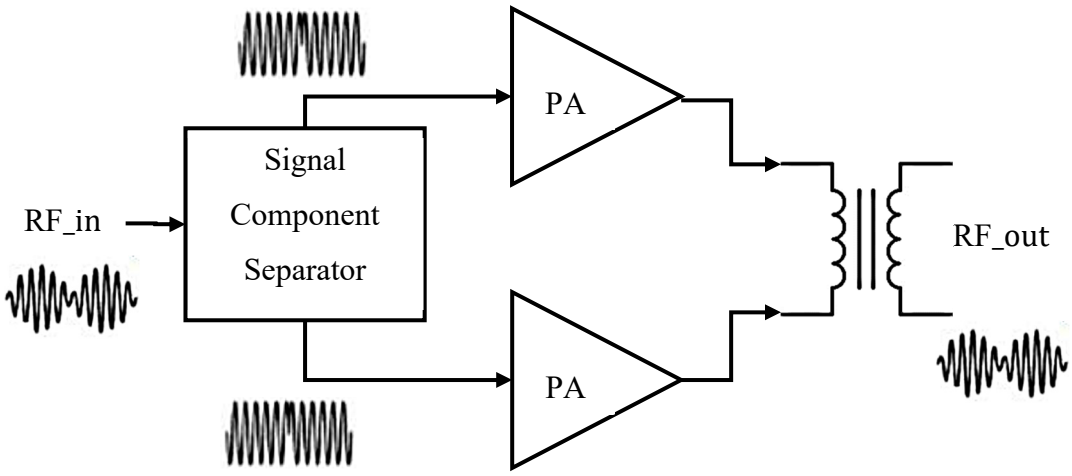


Figure 2.11: The out-phasing PA Architecture [96]

The out-phasing PA is narrowband, similar to ET, EER and DPA. The change in overall system's PAE depends on linear/non-linear class of PA. Furthermore, because system efficiency strongly relies on how the DSP algorithm is organized, simple details like the process, PA class, and frequency are insufficient to accurately explain system PAE.

2.8 Envelope Elimination and Restoration (EER)

Envelope Elimination and Restoration (EER), commonly named as the Kahn-TX, is the first kind of dynamic power supply with which the PAs under OBO are powered by a PA to enhance their efficiency [21]. The RF(Input) is split into two channels, as shown in Figure 2.12. The envelope is retrieved by the envelope detector (ED) to create the amplitude modulation signal, and the limiter will provide the phase modulation signal by removing the envelope from the input signal. The envelope amplifier will effectively enhance the first, and a switching PA will amplify the second. The phase modulation envelope will then be restored by the amplitude modulation signal, amplifying the original input signal in the process [21, 98].

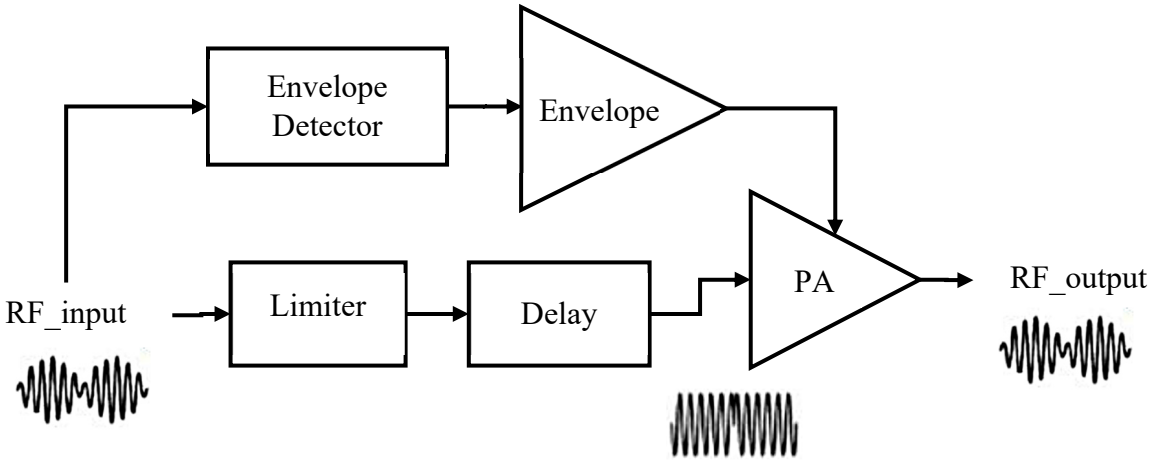


Figure 2.12: Traditional EER Architecture [21]

Unfortunately, the low-frequency envelope modulator limits the PA's bandwidth, making this approach only suitable for narrowband applications [99]. However, utilizing certain methods, such as a “hybrid EER” design where the PA envelopes pr covers only the modulation signal's bandwidth as compared to the phase-modulated signal's bandwidth, it may be possible to increase the bandwidth of the EER. EER also has a limited linearity because of a number of causes, such as the envelope and phase modulated signal, and supply modulator’s phase-phase mismatch. It also makes it more power-hungry, making it completely inappropriate for designing ultra-low power devices. However, a number of approaches, including as pre-distortion, envelope feedback, and phase lock loop (PLL), have been proposed in the literature to improve its linearity [100].

2.9 Envelope Tracking PA Design

Envelope Tracking (ET) has been considered as a key solution of PA design for amplification of signals with increased PAPR. The idea was first put up in the 1930s as a solution to the issue of extremely high-power AM broadcast transmitters coupled with

inadequate energy efficiency. A modulator for adjusting the PA power supply in accordance with the baseband's envelope is incorporated into the dynamic supply, commonly named as ET, a technique for efficiency improvement that is based on the more established EER architecture that was first proposed in 1952. Fundamentally, the primary concept of ET, a version of EER, is dynamically adjusting the voltage supply to the envelope of the RF(Input). Figure 2.13 shows a generalized schematic of the ET PA.

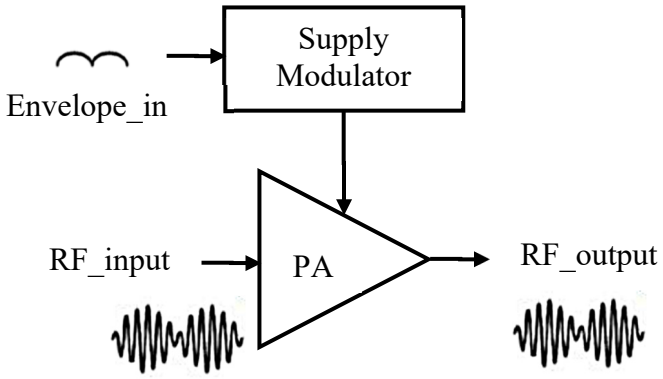


Figure 2.13: Representation of the simplified ET architecture

The performance of the PA will significantly rise as a function of tracking the input signal's envelope since this method keeps the PA mostly close to compression. The technology is utilized in a wide range of devices, including smartphone-handsets, broadcast transmitters, cellular base-stations, and a considerably more. Furthermore, irrespective of the fact that ET is sometimes considered to be a recent technology, the idea has really been around for quite some time.

2.9.1 The Conventional ET-PA Architecture

Figure 2.14 illustrates the basic transmitter setup used by the traditional ET. The power for the RF PA comes from a fixed source voltage, which is often a switch mode supplied power, to achieve the highest level of efficiency. The RF generator powers a preamp, which in turn powers the RF PA. Due to the OFDM with BPSK modulation technology, it is thought to be a suitable technique for current technologies like HaLow, NB-IoT, and LoRA.

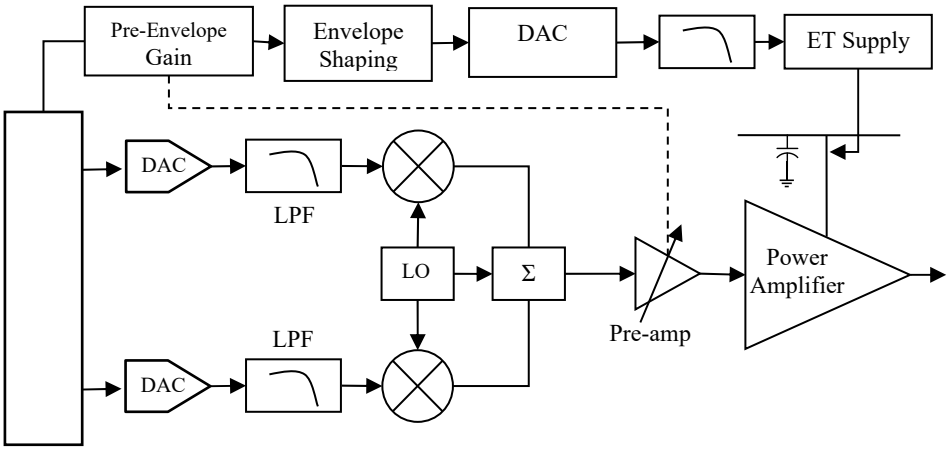
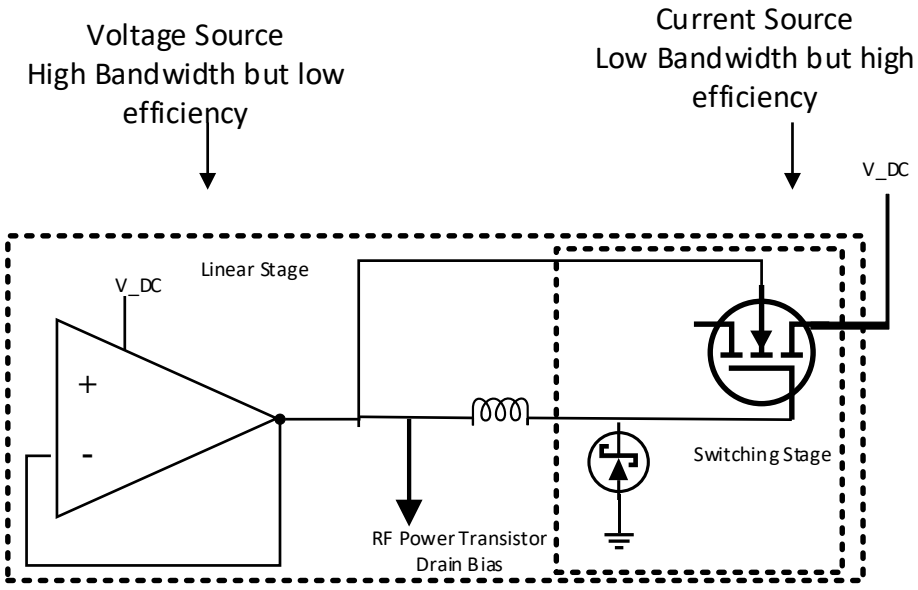


Figure 2.14: Conventional ET architecture with high knee voltage supply modulator design [101]

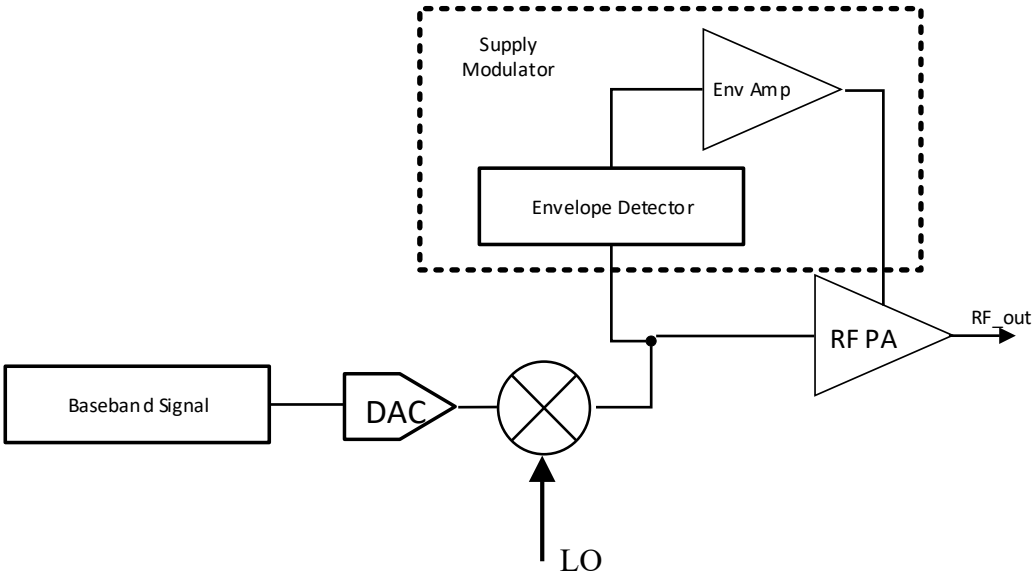
There are two kinds of frequently applicable architectures for ET-PA's design. First one consists of two stages. The linear stage is used to supply adequate voltage source for wideband and a switching stage to provide efficient current supply. This architecture consumes relatively high power due to its nature of static power dissipation which is independent of frequency, depends on voltage [102] and is suitable for base stations with wideband transmitters [103].

For ET design, PA's there are two different types of frequently used architectures. The first one has two phases. A switching stage is utilized to produce an effective current supply, and the linear stage is used to give a sufficient voltage-source for wide-band. This

design consumes a lot of power because of its static power dissipation characteristic [102]. This is appropriate for wideband base stations and is frequency and voltage-independent too. [103]. Figure 2.15(a) shows a simplified two stage ET supply diagram having linear and switching stages used with RF-PA. Second architecture consists of ET-PA system with envelope signal supplied by digital baseband. The supply modulator usually consumes less supply but faces linearity issues. Figure 2.15(b) shows the simplified ET PA system with envelope signal provided by ED [101]. When it comes to improving efficiency, RF PAs use this ED technique to form ET PA. As it becomes a much larger problem due to concern about battery life and environmentally friendly operation, it allows significant advancements to be achieved in form of PAE.



(a) Conventional two-stage ET supply architecture



(b) ET PA system using an ED

Figure 2.15: (a) Conventional two-stage ET supply architecture with linear and switching stages for RF PA is simplified (b) ET PA system using an ED to deliver the envelope signal.

The Class B amplifier was first utilized in 1929 by a guy named Lloyd Barton from the University of Arkansas to solve a 500KW AM radio transmitter's energy efficiency issue. Barton eventually went on to design the Class B amplifier. Cellular base station makers revived the technology in the late 1990s in an effort to increase the 3G base stations' energy efficiencies. Now, it may be utilized in smartphones and other portable electronic devices. Applications that explicitly make use of it include cellular 4G LTE networks.

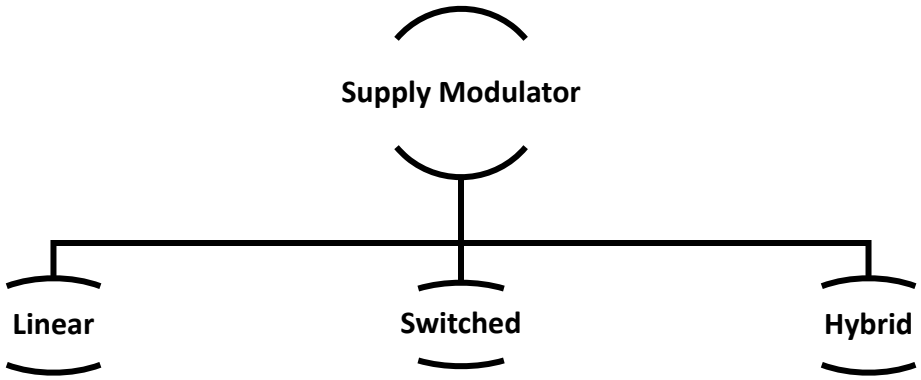


Figure 2.16: Categories of supply modulators for ET-PA

The supply-modulator is often categorized as either a linear or switching kind of modulator, or a mix of the two [104]. While the linear modulator has a greater bandwidth and smaller output ripple (reduced noise), it is less efficient. The switching modulator, however, is often only appropriate for very narrow low bandwidth operation while having a high efficiency with large output ripple. The advantages of switching and linear modulators are combined in a hybrid modulator, which consists of a wideband linear modulator and a high-efficiency switching amplifier. Low-frequency components are handled by the former, while the latter is in charge of high-frequency components. Additionally, the switching noise (ripple) that is often produced by the switching modulator is reduced by the linear modulator [105]. The performance of these supply modulators is critical in determining the ET-overall PA's performance in terms of overall efficiency, linearity, and modulation bandwidth. The deployment of ET in commercial systems is constrained by the difficulties in attaining the necessary performance in terms of modulation bandwidth, efficiency, and output voltage ripple, despite vast and continuing research on supply modulator design [106-108]. Despite being one of the most effective supply modulator kinds, switched modulators naturally create a large amount of ripple voltage. Filtering this ripple results in large losses, particularly when employing high order filters [60], and it also lowers the modulation bandwidth that can be achieved at a given

switching frequency. To lessen the impact of the output ripple, adopting digital pre-distortion (DPD) or bending the envelope may be an excellent choice.

Table 2.3: Performance evaluation of various classification of supply modulators

Supply Modulator / Category	Linear	Switched	Hybrid
Bandwidth	Narrowband	Narrowband	Wideband
Complexity	Simple	Medium	High
Linearity	High	Medium	High
Efficiency	Medium	High	Medium
Output Ripples	Low	High	Medium

2.9.2 ET PA Design Trends

Signal shaping may improve efficiency and linearity, which is another key feature of ET. The main concept behind ET is to reduce the voltage supplied to the PA in order to follow the input envelope. As a result, the voltage supplied is decreased depending on the input signal's envelope without impacting the RF signal, keeping the PA compressed for the majority of the time. The linearity of the PA decreases when the PA is pushed more toward compression to provide optimum efficiency. Therefore, it is presumed that adding DPD is necessary to linearize the ET-PA performance to levels that are acceptable [109]. As long as the supply modulator and PA are equally effective, high efficiency in the ET method may be produced. This occurs as result of the fact that the PA efficiency (η_{PA}) and supply modulator efficiency (η_{supply}) are simply multiplied to get the instantaneous efficiency of the ET system [110-112].

$$\eta_{ET} = \eta_{supply} . \eta_{PA} \qquad (2.4)$$

Due to the OFDM with BPSK modulation technology, it is thought to be a suitable technique for current technologies like NB-IoT, HaLow, and LoRA. It might improve the general effectiveness of PA intended for long-distance communication. Amplifiers in general have a range in which they can function relatively linear, but at a certain input level, compression becomes an issue. The output of the amplifier cannot meet the input signal demand and begins to drop. An RF amplifier operates most efficiently when it is really executing compression. This is acceptable for the signals like the frequency-modulated signals, which don't vary in amplitude. The RF amplifiers are very efficient, resulting in little battery depletion. Despite this, RF filters may be used to filter out harmonics that are produced by operating in compression-region and that occur at frequencies greater than the carrier frequency.

Traditionally, the supply modulator is implemented using a linear regulator, known as linear drop-out (LDO) voltage regulator. But since the linear architecture is inefficient and has a narrow bandwidth and low output-ripple, it is not a good fit for present portable wireless devices. A differential amplifier with a negative feedback circuit connected to the amplifier's output and a power transistor are the three major parts of the fundamental LDO regulator. Depending on the signal envelope, a variable resistor is utilized by the power transistor, that caps the voltage at the PA. A switching (DC-DC) modulator may be used in place of an LDO modulator to create a switching ET architecture. The subsequent design has a high efficiency (over 80%), but since it is switching-based, it induces extra noise and requires a higher switching frequency that will be employed in wireless devices with large data rates [113]. Different variations of the linear and switching ET designs were made possible by these two distinct but still conventional techniques. These hybrids are designed to bypass the switching regulator's bandwidth restriction and the LDO's inferior back-off efficiency. A linear switching regulator link in parallel or series, may be used to build a hybrid regulator, which offers a desired combination of high efficiency, low ripple, and broad bandwidth. Adaptive bias and multimode supply are two more supply modulation techniques that have been documented, although they are not often used for ET implementation [114].

In the case of ED biasing, [115] suggested a method to perfectly tune the preamplifier prior to the detector circuit to increase efficiency and decrease DC power

consumption appropriately. The ET supply unit has been installed in replacement of the DC-DC converter. The CMOS ET supply was adjusted by [116] to increase efficiency of input signal and linearity improvement by second harmonic control at the same time. Nevertheless, coupled to a supply modulator having a high knee voltage for the supply, uses a fair amount of DC power (145mW). For data transfers, the RF generator typically receives I&Q signals, transforms them to analogue form, filters out undesired high-frequency components, and then combines I&Q until the desired frequency is achieved at which these components are added. The RF preamplifier's changeable gain should be noted. To regulate the supply in an ED system biasing and ensure that the handset broadcasts at the proper level for the base station to receive, a signal must be generated. In order to keep the PA functioning efficiently at all times, it operates by quickly adjusting the voltage provided to the PA in accordance to the input signal, supplying a high voltage for strong output powers and a low voltage for weak output powers. In modern communication systems, the change between transmitted power levels happens quickly, therefore applying ET provides significant technological concerns in terms of design, characterization, measurement, and other areas as well. The ET system consists of various subsystems, such as the ET-PA, supply-modulator, baseband generation, envelope detection, and linearization system components, poses a variety of challenges. Traditionally, these interfaces create new issues. For instance, without building a whole ET-PA system, it is difficult to design a MOS functioning in an emulated PA environment, as required in a traditional PA design. A comprehensive comparison of the known ET design differences from the most recent survey is provided in Table 2.4. Although they are not considered as the major techniques for implementing ET, other supply modulation schemes that have been detailed, such as multi-mode supply and adaptive bias supply, both have also been included [75].

Table 2.4: Detail comparison of linear and switching ET supply modulator (regulator) variant design [75]

Regulator Variant	Specifications
Switching Regulator	• Very limited BW of switching frequency • Large output voltage ripple • Less than 50% output efficiency at low-level of input signals • Greater than 90% regulator efficiency
Classic Linear Regulator	• Up to tens of MHz wideband • Abandoned (neglected) output voltage ripple (mV) • Less than 50% output efficiency at low-level of input signals • Less than 60% regulator efficiency
Parallel Switching and Linear Regulator	• Switching regulator supplies an average power to load • Linear regulator acts as an active filter (linear amplifier) • Up to 70% regulator efficiency
Cascaded Switching and Linear Regulator	• Voltage ripples are smaller than switching regulator but larger than linear regulator • Can adjust both narrow and wide bandwidths • Up to 80% regulator efficiency

2.10 Detection of Harmonics in OFDM Based Systems

Due to the harmonic content, PA efficiency has been constantly in the process of improvement. The procedure primarily involves changing the voltage or drain current at the PA's output [117]. The load at the drain output of the PA is investigated using harmonic tuned loads (HTL) of the bi-harmonic and poly-harmonic load, or more generally, harmonic tuned (HT) loads [118]. HTL, which lessen the aliasing impact of current and voltage waveforms, have boosted HTL-efficiency in PA design. Although the termination of harmonics under load adds design complexity, it considerably improves PA efficiency [119]. FFT has been used to convert the OFDM signal to the frequency domain from the time domain, in order to get the frequency coefficients. Fast Fourier Transform is used to achieve present harmonic detection for a traditional OFDM. Traditional Wavelet Transform (WT) has a significant flaw in that it is computationally inefficient [120]. For the purpose of detecting OFDM harmonics, several state-of-the-art digital communication

algorithms have recently been developed. The DWT may remove noise before harmonics and identify harmonics at an immediate level [121]. If an OFDM signal complies with the Nyquist sampling theorem, it may precisely evaluate each frequency component's specifications. However, there are several reasons why frequency interference offset happens. This causes frequency fluctuation in PAs as a consequence of the short-term shift in frequency oscillator with respect to time. Short-range leakage is a term used to describe the spectrum leakage effect of FFT, which lowers measurement accuracy, causing a non-flat rectangular window. The OFDM harmonic, detection and estimation, have been greatly aided by the fields of digital signal processing and advanced communications. Nevertheless, with reference to the front-end design, the harmonic-mismatch, estimation, and RF circuit designers continue to encounter additional difficulties from harmonic rejection [122].

2.11 Summary of Popular ULP Modern RF PA Design Architectures

Table 2.5 summarizes the ULP Modern RF PA designs in terms of architecture, linearization, efficiency and bandwidth.

Table 2.5: Comparison of popular modern PA design techniques

RF PA	Out-phasing/ LINC	DPA	ET
Architecture	Simple architecture. An out-phasing PA is only incorporated in a power combiner, two parallel amplifiers, and a signal component separator.	Simple architecture. There is no need for complex circuitry to respond to the input RF signal. It is acceptable to combine many PAs from various biasing classes. The Main linear PA and the Peaking non-linear PA make up the standard DPA.	A variety of architectural configurations. Envelope detection may be accomplished in the digital signal processing domain or the analogue domain. Techniques for adaptive biasing as well as switching, linear, and their combinations.
Linearization	Predistortion methods could be utilized to improve the overall linearity of the system.	There are no limitations on how feed-forward and pre-distortion linearization techniques may be used.	Although linearization is achievable, it is challenging since other system components like the regulator's nonlinearities must be taken into consideration.

PAE	Due to losses in passive components, practical efficiency is drastically decreased when compared to theoretical efficiency, hence reducing overall PAE.	Design with high efficiency. The DPA's load-pull architecture, which makes use of $\frac{\lambda}{4}$ microstrips, enables the designer to obtain greater overall PAE at any given frequency range with fewer precise additional circuit solutions. Furthermore, the DPA is almost at its maximum efficiency within the entire OBO range.	High potential for PAE improvement: May result in a PAE may improve by up to 20% compared to other methods.
Design Complexity	There is a need for specific power combiners. It is because common power-combiners like Wilkinson or Hybrid can't perform well enough in out-phasing architecture.	Both lumped and distributed implementation strategies can be used for the impedance divider and the power splitter models. RF route power losses are lower; thanks to the power splitter and combiner unlike an	Have to choose between variety of supply regulators including classic linear, switching, parallel combined, series combined or adaptive supply biased.

		out-phasing PA design.	
Bandwidth	Disadvantage is the narrow and limited bandwidth. The power combiner is the key barrier. Wide-band use is not recommended according to the quarter wavelength impedance transformer's constraints or limitations.	The output's parameters output $\frac{\lambda}{4}$ microstrip impedance inverter impose a restriction on the operational bandwidth.	High: Being appropriate for narrowband due to the ET power supply's ability to precisely follow the modulation envelope and its reported maximum band-width of 40MHz.

2.12 Sub-threshold ULP CMOS Design

A nominal voltage applied to the MOS transistor's gate creates an inverted channel between the drain-to-source to conduct current and controls the majority of the existing carriers. The majority of the substrate's carriers are rejected from the surface immediately below the gate when a low voltage is supplied to the gate. Then, a depletion area is produced beneath the gate by a stationary atom depletion charge. When the MOS device's drain and source are put under voltage, the minority carriers in the depletion layer are induced to propagate by diffusion and generate a drain current. The characteristics of MOS transistors have been explored at a very low current level, which is significant to the design of electronic wrist watches. Studies [123, 124] show that the drain current and gate voltage have an unique exponential relationship. Figure 2.17 depicts the first measurement of a

MOS transistor's drain current below the MOS device threshold voltage. The subthreshold current is the term given to this weak inversion current.

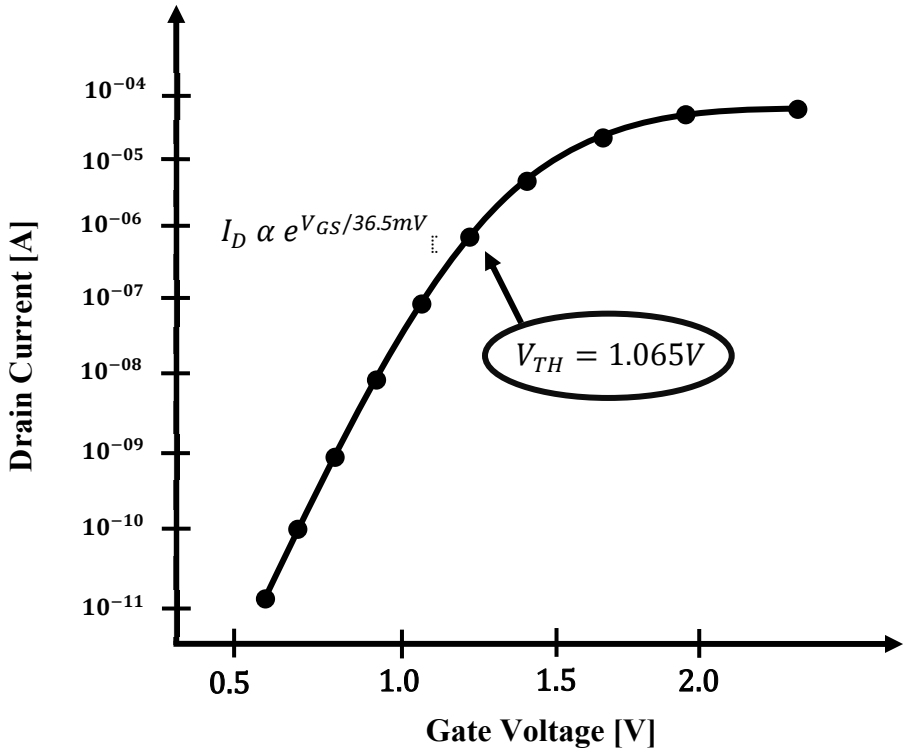


Figure 2.17: The first time a MOS transistor was measured at a very low current (results from Vittoz's notebook) [123, 124]

2.12.1 Subthreshold current

The voltage supplied at which a transistor operates determines its operating region. Strong inversions, moderate inversions, and finally mild inversions occur in the region of operation, when the transistor operates in subthreshold region. Large current drives and a voltage supplied significantly above V_{TH}, the transistor's threshold voltage, define the strong inversion area, commonly named as the super threshold region. In comparison to the super threshold region, the mild inversion has lower current drives and an operating voltage near the V_{TH}. Small current drives and a voltage supplied below V_{TH} define the

weak inversion zone, often referred to as the subthreshold regime. Equations (2.3) and (2.4) illustrates how the transistor behaves in the subthreshold and the super-threshold regions.

$$I_{sub} = \frac{W}{L}\mu_n C_{ox}(m-1)V_T^2\, exp\left(\frac{V_{GS}-V_{TH}}{mV_T}\right)\left(1-exp\left(\frac{-V_{DS}}{V_T}\right)\right) \quad (2.5)$$

$$I_{sup} = \frac{g_{m(sat)}}{1+Rg_{m(sat)}}(V_{DD}-V_{TH}-V_{Pinch}) \quad (2.6)$$

where W and L are the width and length of MOS respectively, C_{ox} is the oxide capacitance, μ_n is the mobility of electrons, m is the subthreshold slope, $g_{m(sat)}$ is the saturation transconductance, R is the resistance at source, V_{Pinch} is the pinch-off voltage, I_{sub} is subthreshold drain current, and I_{sup} is super threshold drain current.

The current flowing from a MOS's source and drain while it is in the subthreshold or weak-inversion region is referred to as subthreshold conduction, commonly named as subthreshold leakage or subthreshold drain current, i.e., when V_{GS} is less than V_{TH}. Leakage current is the flow of incredibly small current in MOS circuits even when the V_{GS} is zero. Figure 2.18 illustrates the subthreshold and super threshold regions of operation. The current is relatively linear in nature in the super threshold zone. The transistor current I_{on} is exponentially correlated with V_{TH} and voltage supplied in the subthreshold region, power, delay, and current matching between two transistors are likewise exponentially dependent on V_{TH} and V_{DD}. There are several difficulties in designing subthreshold circuits, including the exponential relationship. Output voltage swings, soft errors, noise margins, and process variations are some of the characteristics that are influenced by this difficulty. As a result, these factors are crucial for developing energy-efficient subthreshold circuits. When operating the transistor in the super-threshold region, leakage current, often known as subthreshold current, is a kind of unwanted current. However, in terms of subthreshold operation, this current is necessary and subthreshold circuits use leakage current as their conduction current.

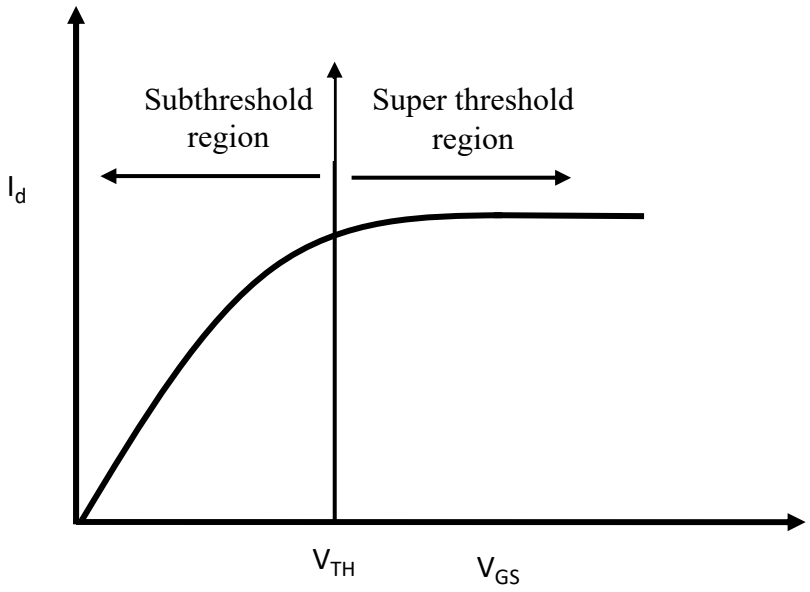


Figure 2.18: Subthreshold and super threshold regions of operation

2.12.2 MOS Inversion Regions

The three inversion regions are strong inversion, moderate inversion, and weak inversion, in which a MOS device would be biased, each allowing different current and transconductance properties. Weak inversion happens when V_{GS} is sufficiently lower than V_{TH} in a MOSFET. The channel is weakly inverted in this region, and primarily the drain diffusion current, causing the drain current to converge to [125]:

$$I_D = I_{D0} e^{\frac{V_{GS}-V_{Th}}{2U_T}} \tag{2.7}$$

where I_{D0} is the CMOS technology current defined by:

$$I_{D0} = 2\mu_n C_{ox} U_T^2 \left(W/L\right) \tag{2.8}$$

where effective channel width is W, while effective channel length is L, μ_n is mobility of electrons (carrier mobility), C_{ox} is the oxide-capacitance, $V_{GS} - V_{Th}$ resembles the overdrive ($\mathbf{V_{OV}}$) and U_T is the thermal voltage defined as $U_T = {kT}/{q}$.

When V_{GS}-V_{TH} exceeds a certain high-level, the channel becomes severely inverted, and drain drift current becomes dominant. The drain current in this location may be stated as [126]:

$$I_D = \frac{1}{2}\mu_n c_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{2.9}$$

A MOS has two distinct operating regions: the weak and strong inversion regions. The moderate inversion refers to the region that exists between these two, and is characterized by both drift and diffusion currents. Moderate inversion is essential for a perfect state-of-the-art ULP-PA design. The inversion coefficient of a transistor may be used to calculate its global inversion region coefficient (IC), and is defined by [125, 126] as:

$$I_D = \frac{I_D}{I_{D0}} = ln^2\left(1 + e^{\frac{V_{GS}-V_{Th}}{2U_T}}\right) \tag{2.10}$$

where the inversion coefficient of a transistor may be used to calculate its global inversion coefficient (IC). IC < 0.1 equates to weak inversion. If the range is 0.1 < IC < 10, the transistor is in moderate inversion, and if the value is more than 10, strong inversion is observed in the transistor. For each inversion region, the requisite V_{GS} and V_{OV} voltages must be determined. Figure 2.19 shows the over-drive voltage (V_{OV}) and the drain-source voltage (V_{DS}), with respect to IC.

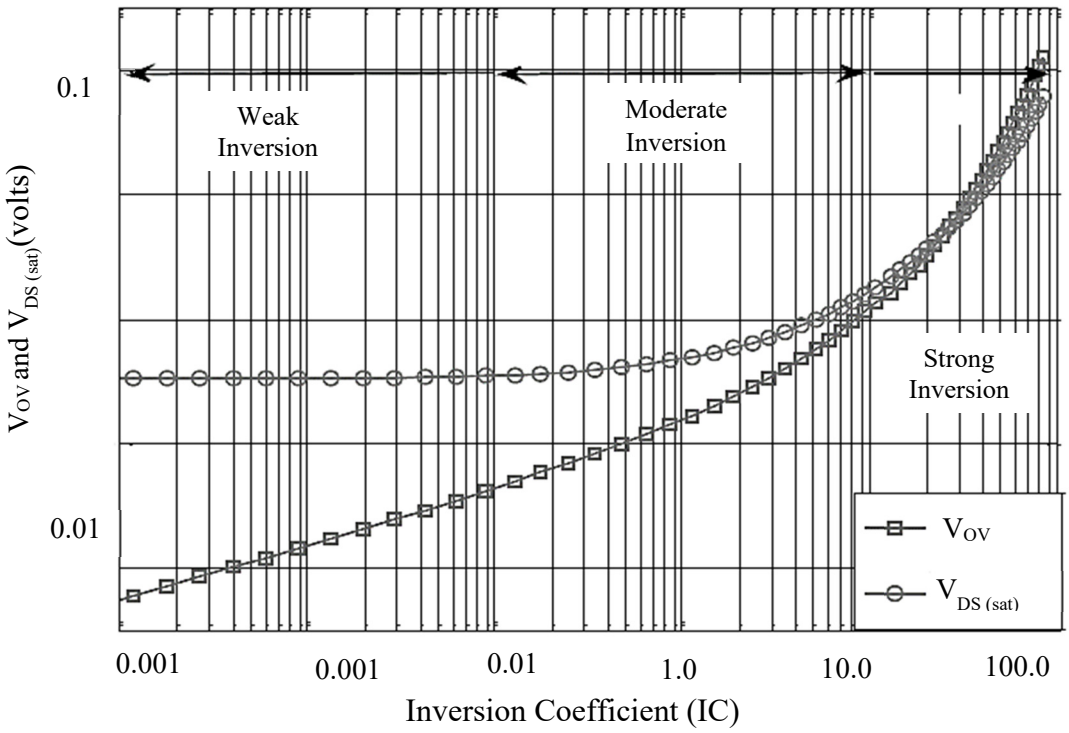


Figure 2.19: The over-drive voltage (V_{OV}) and the drain-source voltage (V_{DS}), with respect to inversion coefficient [127].

2.12.3 DC Power Consumption Sources

A CMOS circuit's power dissipation may be modelled as [128]:

$$Power_{total} = Power_{static} + Power_{dynamic} \tag{2.11}$$

When the following definitions apply:

$$Power_{static} = I_{static} V_{DD} \tag{2.12}$$

$$Power_{dynamic} = \alpha_a C V_{DD}^2 f_{operating} \tag{2.13}$$

where α_a is the activity ratio, or the percentage of transistors that switch on or off in a particular period; C stands for the circuit's capacitance; V_{DD} for the supply voltage; and $f_{operating}$ is for the operating frequency. This would be the clock frequency for a synchronous circuit; however, it is more difficult to specify for an asynchronous circuit. I_{static}, commonly known as leakage, is the supply current seen whenever the circuit is in a steady state and is the static current. Reduce any or all of these elements while maintaining the appropriate performance attributes to achieve low power operation. Reducing V_{DD} may significantly cut power usage since it lowers both static and dynamic power. The maximum frequency of the circuit is lowered as a result of the supply voltage reduction because subthreshold and near-threshold systems operate more slowly. Results from simulations presented in chapters 3 and 4 are used to analyse how supply voltage affects frequency and power usage.

Definition of subthreshold power supply - "If the voltage source powering the circuit is lower than the transistor threshold voltage ($V_{DD} < V_{th}$), the circuit is said to have a subthreshold power supply. Similar to a near-threshold supply, this one has a supply voltage that is within a few hundred mV of the threshold voltage or just slightly over it. The majority of conventional circuits operate in the remaining area, which is known as the super threshold region."

Definition of subthreshold conduction - "The current flowing between a MOS source and drain while it is operating in the weak-inversion sub-threshold region, is referred to as subthreshold conduction, subthreshold leakage, or subthreshold drain current ($V_{GS} < V_{TH}$)." This definition has already been discussed in detail in section 2.11.1.

2.12.4 Investigation of Subthreshold Gates' Characteristics

This section describes how subthreshold logic works at the gate level modelling. The behaviour of a gate at subthreshold is roughly same as super threshold, with the exception that it is much slower and uses a lot less power. Three categories - devices, gates, and logic families - are used to characterize subthreshold logic at the low level in this subsection. A review of previously published publications is done in each situation. Chapters 3 and 4 study a subthreshold gate in depth.

Models for CMOS transistor behaviour below the threshold are put out by [129] and [130]. [131] uses the logical effort concepts to determine the best size in the subthreshold regime. [132] uses a theoretical strategy to achieve lowest energy operation in analogue frontend architecture. At subthreshold, transistor design has also been examined. [133] demonstrated that using ordinary devices is not the best course of action and suggested optimized devices for functioning below the threshold. [134] addressed the subthreshold device scaling. Both articles reach the same conclusion that less doping enhances performance. Although [134] suggests using transistors with longer channel areas than the required minimum. A standard silicon-based MOSFETs created for super threshold applications will be employed as the transistors. The objective was to investigate low-cost subthreshold design applications. So typical CMOS techniques with large volume were used. Adoption would face further obstacles if novel devices or non-standard doping levels were required.

There are two main factors to take into account when selecting an architecture for subthreshold applications. It should be energy efficient first. Utilizing a subthreshold supply is mostly done to save energy. The use of an ineffective architecture shouldn't prevent this. The second factor to take into account is the extreme process variability that is seen while operating below threshold. Variability, particularly intra-die variance, would be reduced with a good subthreshold design. The ease of development must be weighed against these objectives. Even a design with perfect power generation and variation tolerance is of little use if it is impossible to build systems around the same die. This is referred as on-chip design using lumped and transmission parameters.

2.13 ULP Design Biasing Scheme

The new biasing point for achieving ULP for a single transistor will be discussed in this section. The objective is to identify a biasing point in which the transistor has a good transit frequency (bandwidth) and gain while using very little power from a low voltage supplied. The low frequency gain of a CS MOSFET with a current source at the drain is given by g_m/g_{ds}. G_m/I_D represents the transconductance efficiency. Various biasing

schemes [135] with figure-of-merit (FoM) for low-power circuit design have integrated the FoM given by ${g_m}/{I_D} \cdot f_T$. Variation in the V_{DS} has a significant impact on the intrinsic gain (specifically on the G_{DS} of a transistor). To account for the impact of low voltage supplied, the effect of V_{DS} on the intrinsic gain must be incorporated. As a result, the modified FoM utilized here is defined in equation 2.12 as transconductance efficiency as a product (g_m/I_D) is the intrinsic-gain (g_m/g_{ds}), and transit-frequency (f_T) [127, 136, 137].

$$Biasing\ Metric_{(ULP)} = \left({g_m}/{I_D}\right).\left({g_m}/{g_{ds}}\right).f_T \tag{2.14}$$

The following are some of the benefits of biasing transistors in weak and moderate inversion zones (regions):

- The necessary bias voltages ($V_{DS(sat)}$) are lower than in strong inversion regions, allowing for low power design.
- The transconductance efficiency, $\frac{g_m}{I_D}$, is higher, allowing for low-power design.
- The intrinsic gain, $\frac{g_m}{g_{ds}}$, is larger, then drops abruptly in the strong inversion region, allowing for high gain low power solutions.

2.13.1 Efficiency of Biasing Scheme g_m/I_D – The Transconductance Efficiency

This section examines the impact of V_{DS} variation on the g_m/I_D. An effective method, for designing analogue MOS circuits with low power, is to use the ratio of transconductance to drain current (g_m/I_D) [138]. The equation for g_m/I_D as a function of IC is given by [139]:

$$\frac{g_m}{I_D} = \frac{1}{U_T}\,\frac{2}{1+\sqrt{4IC+1}} \tag{2.15}$$

Due to channel length modulation, when V_{DS} is lowered, the attainable I_D and, as a result, the device's g_m lowers. The I_D and g_m are both lowered by the same proportion; therefore, the g_m/I_D ratio remains almost constant for varied V_{DS} levels. Figure 2.20 shows the simulation results for the g_m/I_D curve for two V_{DS} values in relation to the IC for 65-nm, 90nm, 130nm, and 180nm technologies in CMOS. A 90nm graph compilation has been shown as an example (this is a similar behaviour for 65-nm CMOS technology).

Interestingly, the g_m/I_D trend does not vary even by doing variations incorporated in V_{DS}. This is applicable for all CMOS technologies. The transconductance efficiency reaches a maximum of $1/U_T$ in the deep-weak inversion region, as can be observed. At the middle of the moderate inversion region, efficiency reaches 0.5 of its maximum and drops with $\frac{1}{\sqrt{IC}}$ in the strong inversion region.

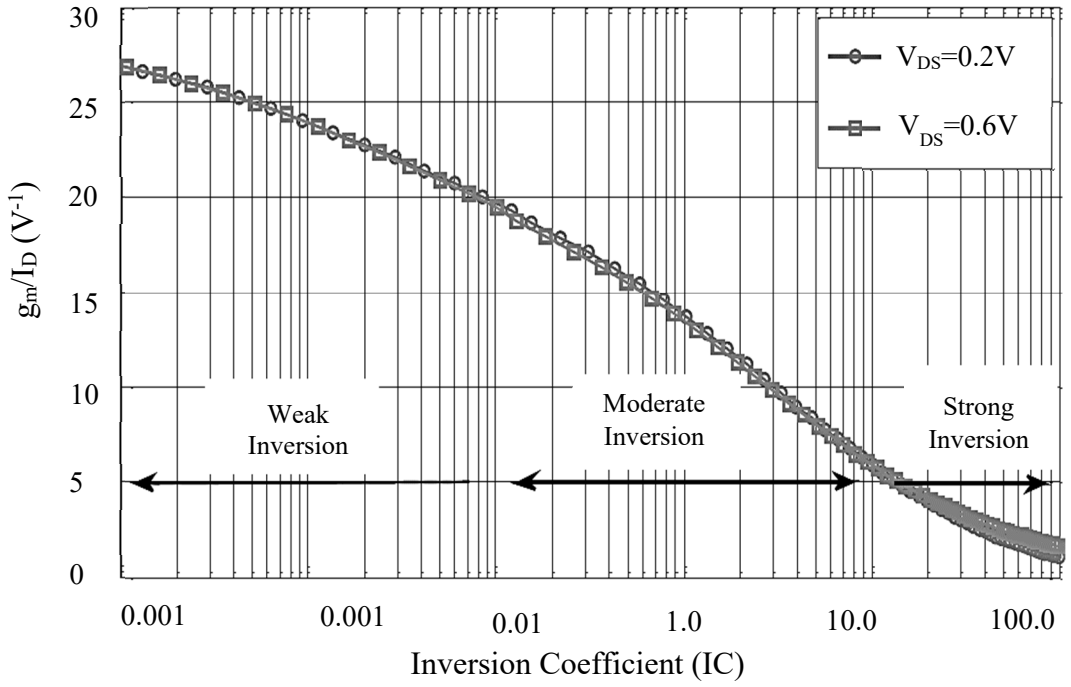


Figure 2.20: The g_m/I_D curve for two V_{DS} values as simulated using nanoscale CMOS technology [127]

2.14 Conclusion

This chapter has highlighted the major studies being conducted on high efficiency PA design in academia. According to the aforementioned literature review, it is evident that numerous approaches have been researched and tested in order to enhance and preserve great performance efficiency compared to OBO and also to other crucial factors like maintaining output power, bandwidth, and ULP consumption.

DPA should be replaced by class-AB, according to history. Modern DPA is a load-modulation design that includes dynamic load-impedance modification for optimum performance. In this instance, the load has been sent to the main amplifier after modulation has been made, or switched to $2R_{opt}$ from $R_{opt}/2$. The DPA architecture is undoubtedly a straightforward design, and industry continues to be drawn to it because it is a straightforward RF(Input) & RF(output) architecture. Over 6 dB OBO, the traditional DPA can achieve excellent efficiency. Although it adds to the complexity of the circuit, the input attenuation technique allows for easy provision of phase correction, which is crucial for certain device technologies, and the ability to change the relative phase between the main and peaking amplifier's input. The load-modulation approach is the most efficient way to control the peaking amplifier's basic current and turn-on behaviour. This prevents the peaking amplifier from turning on too soon or too late depending on whether the primary amplifier is saturated or over compressed.

In the case of ET systems, which assures to provide a high-bandwidth solution, the constraints include the size of the DC supply-modulator and the modulator's possible bandwidth. Among the many alternative improvement methods that have been created, the ET strategy is one of the most promising prospective strategies to address these challenges. A number of supply modulator techniques are found and contrasted in terms of their benefits and drawbacks before the ET technique is implemented.

The strong inversion regime is explored in regard to the current flow mechanism and the exponential relationship between the voltage and current at gate and drain respectively of MOS transistors in the subthreshold regions. Subthreshold circuits originally came to light in the analogue world, but didn't catch on in the digital world until the late 1990s. Several subthreshold measures have been put into action afterwards, using standard DSM technologies. The impact of operational differences on circuit behaviour is then addressed. Very few ULP design techniques, from various literatures, have been discussed to improve the MOS device characteristics.

At subthreshold, transistor design has also been examined. [133] demonstrated that using ordinary devices is not the best course of action and suggested optimized devices for functioning below the threshold. [134] looked at subthreshold device scaling. Although [134] also suggests the usage of transistors with larger than minimum length channel

sections, both studies (contributions to this study) reach the same conclusion that lower doping enhances performance. Transistors with a standard silicon base and subthreshold applications will be employed in this thesis. The objective was to investigate low-cost subthreshold design applications. So typical CMOS techniques with large volume were used. Adoption would face further obstacles if novel devices or non-standard doping levels were required.

A number of factors were used to assess the CMOS PA's performance. PAE, output power, power gain, power consumption, and linearity, are a PA design's key considerations. These characteristics always include trade-offs, which make PA design for CMOS downscaling difficult.

CHAPTER 3

RESEARCH METHODOLOGY

3.1 Overview and Research Epistemology

A variety of well-known CMOS PA designs are already addressed in chapter 2, that have been adopted to increase efficiency under low power conditions. A comprehensive understanding and model underpin the design and operation of a CMOS RF PA. The research epistemology for a CMOS RF PA involves a rigorous and iterative process of theoretical analysis, simulation, and experimental validation to ensure the development of a high-efficient and linear design. This chapter proposes methodology of two novel high-efficient PA designs as under:

- Design and optimization of ULP Doherty power amplifier (DPA) with fixed inter-stage capacitances for short-range and low power IEEE 802.15.4 WPAN standard.
- Design and optimization of Envelope Tracking (ET) supply bias with cascoded cells terminated as class-F ULP PA for long-range and low power IEEE 802.11ah WLAN standard.

The research uses simulation tools to model the behaviour of the CMOS RF PA under different operating conditions and to optimize its performance. This involves a combination of circuit simulation and layout design tool, for electromagnetic simulations. Section 3.2 to 3.4 shows the design and optimization of ULP DPA, while section 3.5 to 3.8 shows the design and optimization of ET supply bias ULP PA. Section 3.9 concludes the methodology by summarizing the design methods for both proposed PA architectures.

3.2 Design and Optimization of ULP Doherty Power Amplifier (DPA) with Fixed Inter-stage Capacitances for Short-Range and Low Power IEEE 802.15.4 WPAN standard

The fundamental idea and behaviour behind DPA are emphasized as one of the most promising methods for increasing efficiency under low power conditions. In addition to the traditional DPA implementation, many advanced DPA implementations, such as input attenuation and bias adaptation are introduced.

This major objective of this section is to demonstrate the design of a device modelling method that eliminates the impacts of reactive parasitic components at 2.4 GHz frequency operation by using both ideal models and real-supplied models under low power consumption. To guarantee that models can be employed in DPA design, the topic continues to address model validation. Additionally, using the Classical DPA as a basis of reference.

This section has included the Doherty implementation simulation operations with the aim of highlighting the significant variations between them. The ideal device model which is created using CAD design tool analogue library, is shown first, and the real device model created by the real component-based library of 65-nm CMOS technology is shown next to the ideal component-based design. The study will later go through the simulation findings of DPA implementation. The results from the DPA designed technique will then be compared and summarized using a validated device model.

3.3 The Development of DPA Model Using Ideal Components

The initiation involves defining notations for main amplifier current (Im) and peaking amplifier current (I_p). These fundamental currents (I_m and I_p) of the main and peaking sources are used to calculate the governing equations of the DPA, and the ideal impedance of the main source at peak power, R_{opt}, using the simplified schematic illustrated in Figure 3.1 [140]. This investigation contributes to a qualitative understanding of the DPA's efficiency increase. Generally, the amplitudes of the input and output signals

have nonlinear effects on both the main and peaking currents. The basic current profiles for the main and peaking transistors are represented by the equations:

$$I_m(v_{in}) = \begin{cases} v_{in}.I_M & 0 < v_{in} < 1 \\ I_M & v_{in} > 1 \\ 0 & elsewhere \end{cases} \quad (3.1)$$

$$I_p(v_{in}) = \begin{cases} 2(v_{in} - 0.5).I_P & k < v_{in} < 1 \\ I_P & v_{in} > 1 \\ 0 & elsewhere \end{cases} \quad (3.2)$$

where $v_{in} = k$ is the breakpoint where the current starts to flow from the peaking source. It is also the saturation point for the main source (v_{in} shows the normalized input voltage from main current source and k = 1/2 for a classic DPA architecture). The peaking device's voltage and current must lag by 90^0 since it is believed that the currents are coupled in phase at the output combiner. The impedance inverter's ABCD-parameters, which link the current and voltage components at its input and output terminals, must be used to evaluate the circuit. Therefore:

$$\begin{pmatrix} V_2 \\ I_2 \end{pmatrix} = \begin{pmatrix} 0 & -jZ_o \\ -\frac{j}{Z_o} & 0 \end{pmatrix} \begin{pmatrix} V_1 \\ I_1 \end{pmatrix} \quad (3.3)$$

where (V_1, I_1) and (V_2, I_2) are input and output ports of main and peaking amplifiers respectively.

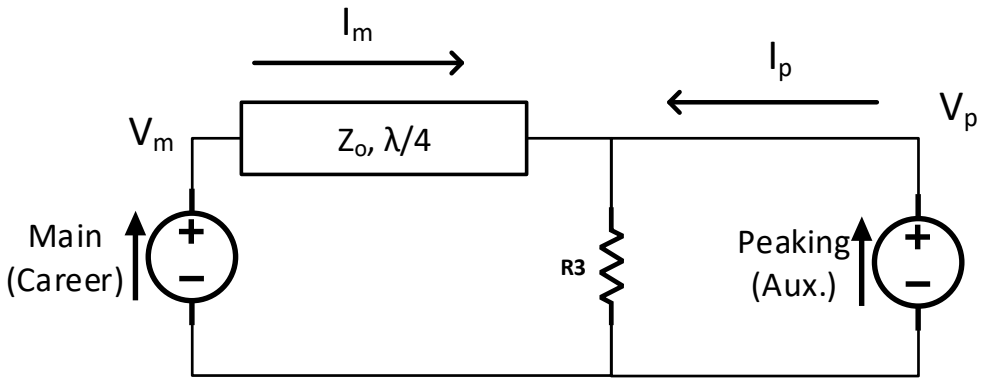


Figure 3.1: DPA representation with λ/4 Impedance inverter [140]

3.3.1 The Ideal Power Divider and Combiner Models

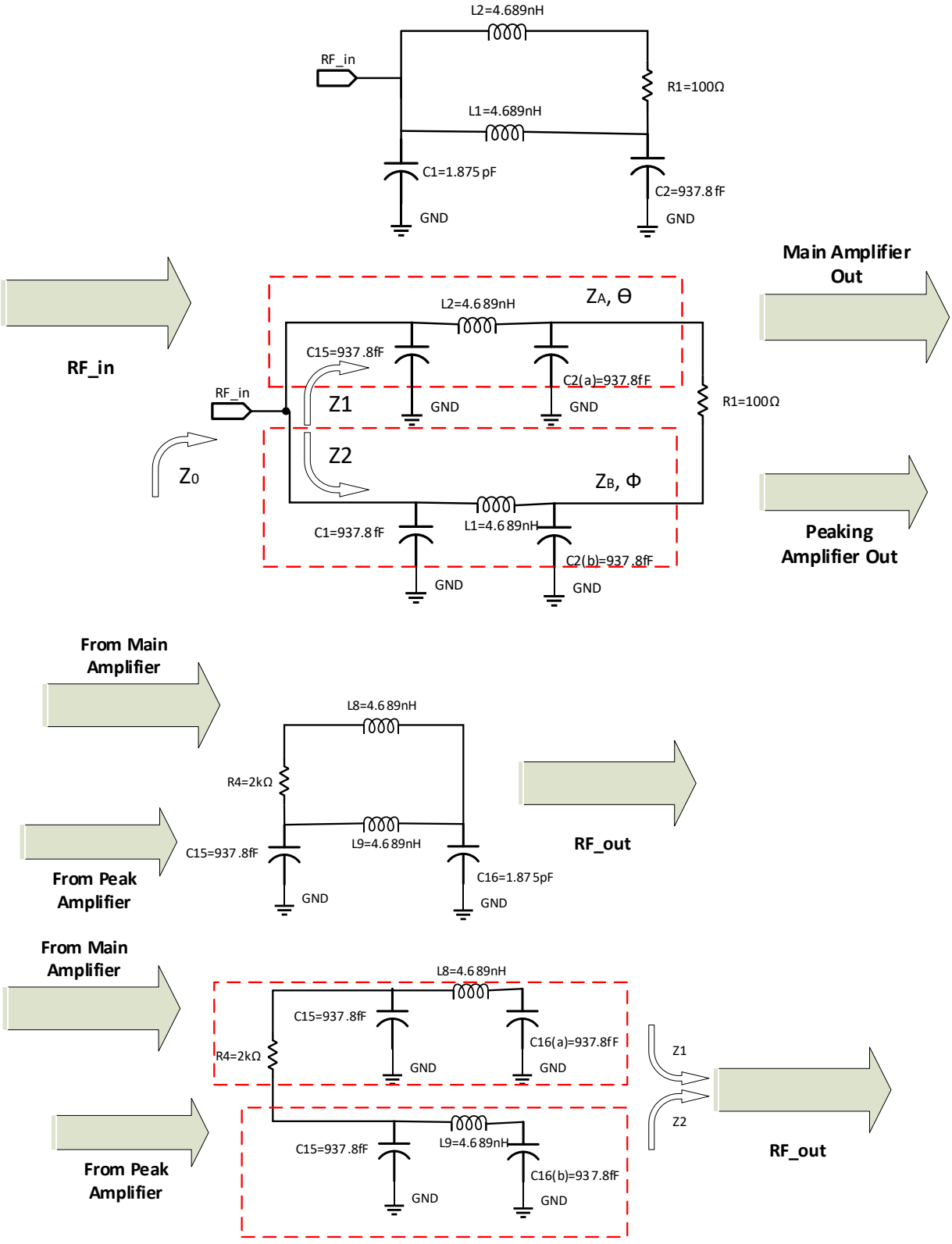
The main and peaking amplifiers are often pre-matched using a free scale. These two amplifiers perform operation with a 90^0 phase-difference. This is accomplished with a Wilkinson power divider or a hybrid splitter with a 90^0 phase-shift. Furthermore, after being amplified, the two signals must be mixed once again. At the main amplifier's output, a 90^o transmission line is used to accomplish this division. The main PA is theoretically biased as class-B, but in practical, we chose to bias in class-AB. The peaking amplifier has been biased in class-C. When the signal level of DPA is low (back-off mode), the peaking amplifier is off and only the main amplifier is operational. Means the biasing point of class-C is further slightly lower than the pinch-off point. This is the secret sauce which improves the efficiency of DPA. Another important and critical part of DPA is Doherty combiner or the power combiner circuit [141]. It is accomplished by a second 90^o transmission line, which typically has a characteristic impedance of 50Ω divided by square root of 2. A Doherty combiner circuit's role is to transform a load's 50Ω impedance to a 25Ω impedance at the DPA's power combining node. It links the main amplifier, which has a 100Ω impedance, to the Doherty node. As long as the amplifier is turned off, the impedance level remains constant. The peaking amplifier signifies a higher impedance to its combining nodes, which is another crucial point. When the main amplifier's input signal level rises to its saturation level, the peaking PA begins to create power, nevertheless, on

the other side, this phenomenon is referred to as the impact of load-modulation since it also causes the main amplifier's output impedance to rise [142].

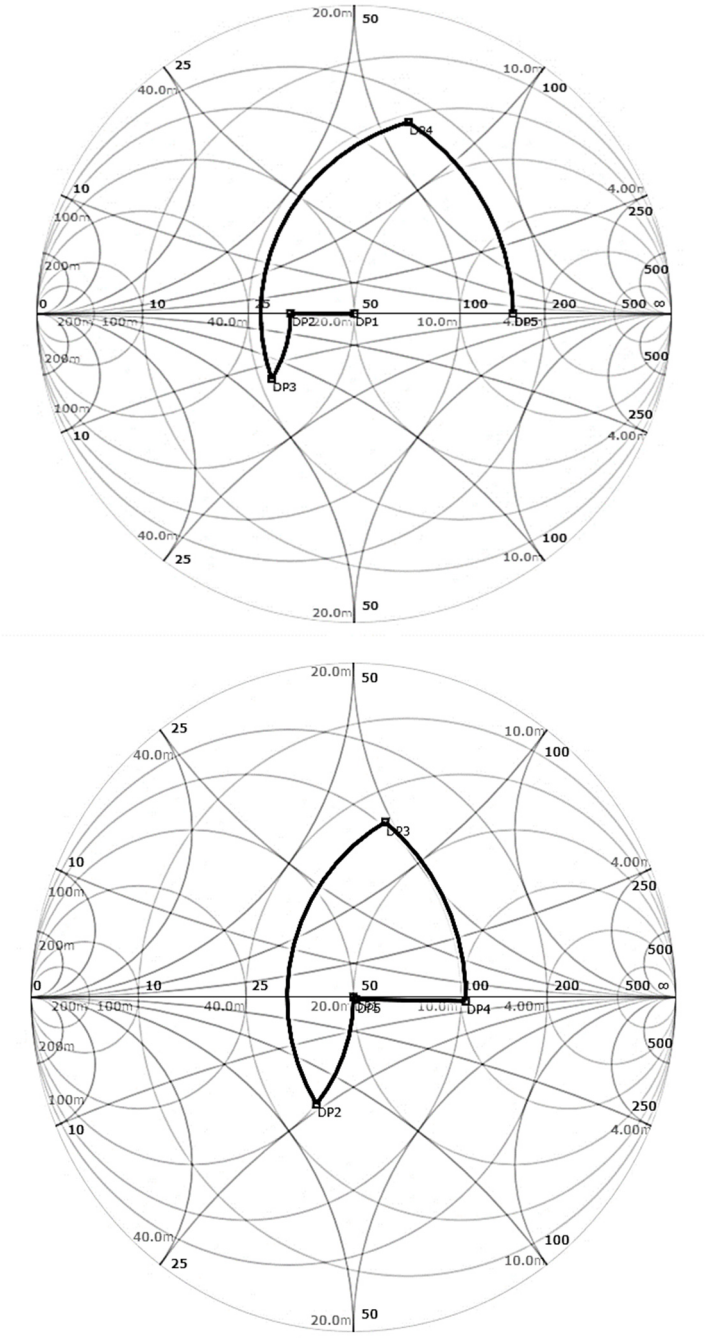
The analogue BPSK has modulation index of 0.5 which offers output power of 0 dBm (1mW) for around 10m range. For equal division of power, a Wilkinson power divider model has been designed using equivalent lumped parameters. The power combiner ideal model operates at 2.4 GHz band with two output ports dividing the power equally. This is because inductive splitters, which cause a 90° phase shift between the two signals, are employed to prevent power loss. The design has been developed for low power purposes in line to DPA architecture requirements. The input signal is divided into two signals with equal in amplitude but with a 90º phase using the Wilkinson power divider. Two transmission lines measuring a quarter of a wavelength and a resistor linked in between the output ports make up the most basic configuration. The usage of a single band with a power divider demands excellent impedance matching. Both the peaking amplifier and the main amplifier are intended to be loaded at Z_0 Transmission lines input impedance has been calculated using both equal and unequal power divider approaches in a number of older designs. In [143], and [144], there were found symmetric and asymmetric lumped element power divider schemes..

The peaking and main amplifiers both use the equal power divider concept, it turns into a lossless model if the ports of the Wilkinson power divider are matched. Thus, ideal for creating a low-power divider model. A comparable circuit is created with this technology using the same methodology. Pi-network does the 90º phase shift at one of the ports. This work was previously completed using the same BiCMOS technology [145]. In order to attain 90º phase, Figure 3.2(a) depicts an analogous lumped circuit model developed as a pi-network [146]. Setting $Z_o = 50\Omega$ for a perfect matching, with the following RLC parameters and tuned at 2.4 GHz frequency, the distributed realization may be seen as: $R = 2Z_o = 100\Omega$, $L = \frac{50(\sqrt{2})}{2\pi(2.4\text{GHz})} = 4.689\text{nH}$ and $C = \frac{1}{2\pi[50(\sqrt{2})](2.4GHz)} = 937.8\text{fF}$. In addition, acceptable for an insertion loss of around -3 dB, which the optimal value, given by:

$$Insertion\ loss = 10log_{10}\left(\frac{input\ power}{output\ power}\right) = 10log_{10}\left(\frac{1}{2}\right) \qquad (3.4)$$



(a) Equivalent RLC circuit model



(b) Input and Output matching for ideal component (analogue library)

Figure 3.2: (a) Equivalent RLC circuit model and (b) Impedance matching using the Smith chart for the lumped parameters of the power combiner and divider models [146]

The $\lambda/4$ transmission line equals $\lambda/4 = \sqrt{2}Z_o = \sqrt{2}(100) = 70.71\Omega$ for our scenario, where we need to completely match at 50Ω. The equivalent lumped parameters equate the transmission line effect at input and output of peaking and main power amplifiers respectively. Figure 3.2(b) shows the smith chart behaviour which starts from the right as the impedance gets high due to parallel effect of transmission line which behave almost an open-circuit, and the supply frequency has reached the resonant value due to calculated RLC parameters. The standard 50Ω value, for our case, is targeted to be reached using very precise steps. The overall system is said to be normalized when actual impedance is divisible by the system impedance, which makes it usable for this designed equivalent transmission line. The transmission line does not represent a purely resistive line, which is even not possible for the case of equivalent transmission line. It starts with the parallel effect of inductance, and then rotating the other way down to the series capacitance which gets closer to the system normalized value of equivalent quarter wave transmission line and it is defined as equivalent lumped parameter for this case. Due to the fact that this is a narrowband circuit, additional cascade with factor less than 1 is prevented as shown in the traditional previous method [147]. By initially employing equal power division and the transmission line theory (theoretical analysis), it is possible to determine the impedance of two ports. The total impedances of Z_1 and Z_2 may be represented as total admittances of Y_1 and Y_2, since the admittance of transmission lines are identical for both. In brief, it is given by $Y_1 = Y_2 = Y_A cot\theta \frac{Y_0 + Y_A tan\theta}{Y_A cot\theta + jY_0}$ [143]. We precisely and alternatively study the impedances on Smith chart which has a characteristic impedance of 50Ω, a frequency band of 40 MHz, and an operating frequency of 2.4GHz. Smith chart in Figure 3.2(b) verifies the measured values using the aforementioned tuned scale once which matches identically. $S_{11} = S_{22}$, $S_{21} = S_{12}$, and $S_{13}=S_{31}$, all are symmetrical, equal and balanced. Figure 3.3 illustrates the ideal model findings, with S_{11} = -87.8 dB, $S_{22} = S_{33}$ = -96.1 dB, and S_{12} = -3.01 dB, reflecting an equal split of the power divider. Valid also for insertion losses that are close to the optimal value of -3 dB.

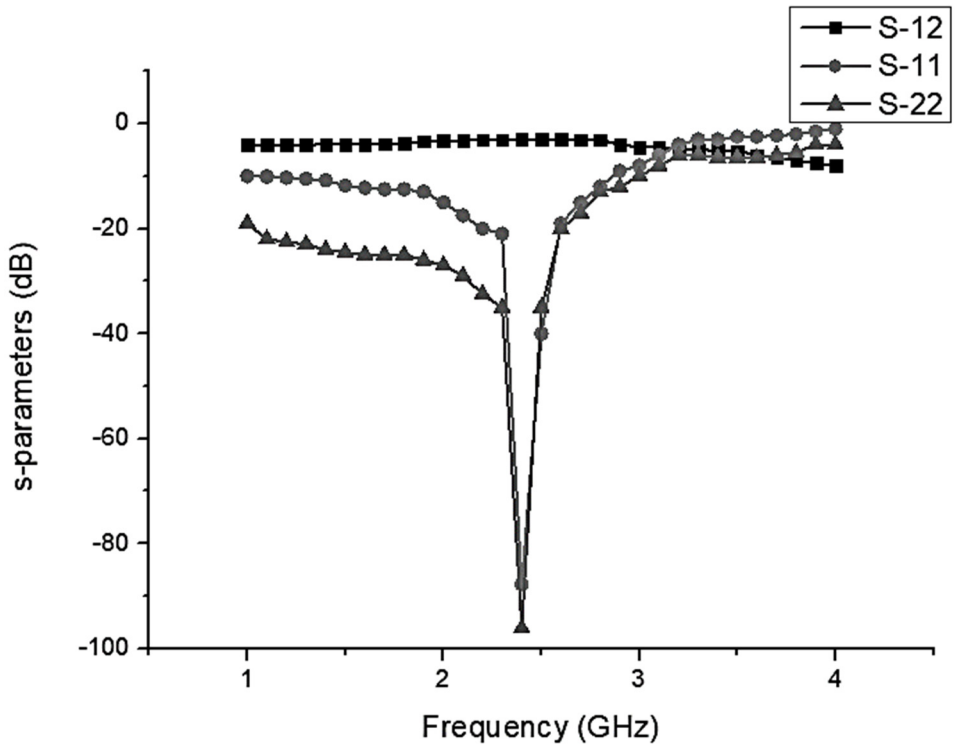


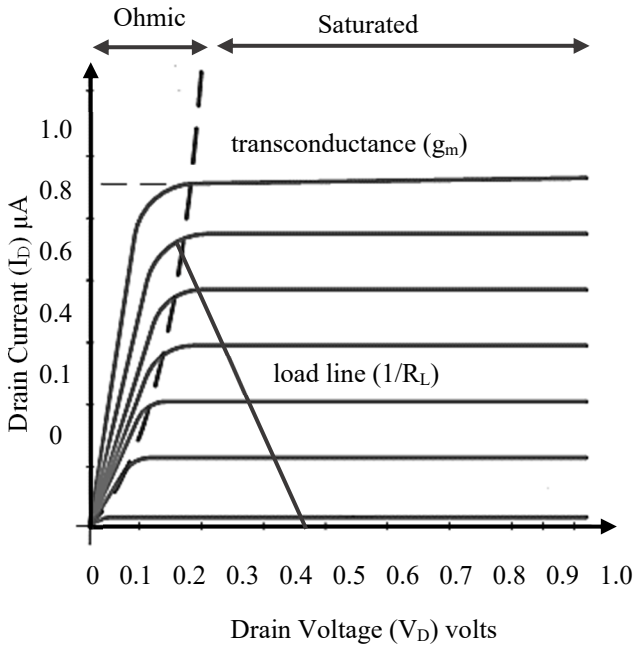
Figure 3.3: Input return loss (S_{11}), insertion loss (S_{12}) and output return loss (S_{22}) for power divider ideal circuit model

3.3.2 Traditional Class-AB PA Model Validation and Load line Analysis using CAD Tool Analogue Library

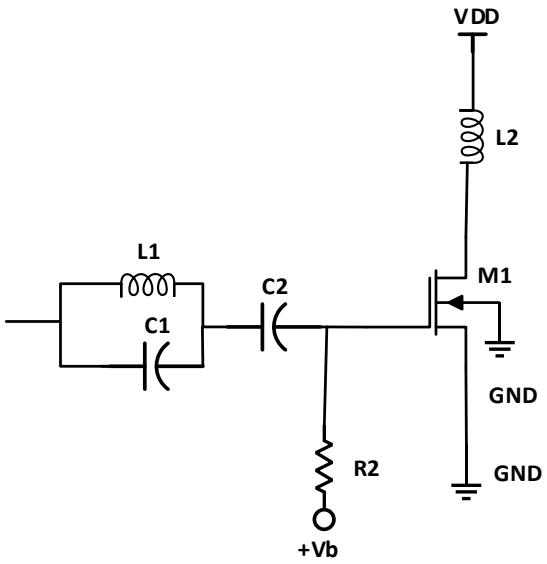
The first step entails modelling the nonlinear transconductance. This is how the transistor switches on when a certain threshold voltage is attained. Modelling of this is significant since large signals have a tendency to break this threshold region, causing the input signal to be rectified. Once the required model is achieved, the quotient-point is switched back to subthreshold region, keeping the output waveform constant. Figure 3.4(a) is the actual mechanism that PA designers exploit to change the class of operation and also employ technique under g_m/I_D mechanism. At the output of PA, there's a knee voltage where the transistor enters the saturation region after some threshold is exceeded, and ideally, this is near zero. And the external load-impedance that is supplied to the device

restricts the load line, which in turn determines the trajectory of the voltage and current swing on the transistor. As a result, the voltage and current are forced to adopt values that are valid points on the device's load line.

Now, in real transistors, the turn-on portions of these curves are either exponential or square law in nature, but to realize the classical PA waveforms, these regions really need to be idealized, which is part of the reason that it's so hard to achieve this ideal operation and practice. Nevertheless, implementing these features in the circuit simulator is rather simple. Without any of the complexity brought on by reactive parasitic components such nonlinear input and output capacitance, CAD tool analogue library components accurately mirrored the largely ideal transconductive nature of a typical RF device, as shown in Figure 3.4(b). The ideal sources are used to design the main and peaking amplifiers and discrete components except of M1 and M2 which belong to 65-nm RF-nMOS analogue library. L1||C1 makes up the resonant current to oscillate the input energy. C2 acts as a DC block while L2 keeps the DC level equal to V_{DD}. The device is biased on subthreshold voltage ($+V_b$) in weak inversion region to reduce DC power consumption.



(a) DC-plot of nonlinear parameters



(b) The Class-B PA

Figure 3.4: (a) DC-plot of nonlinear parameters generated by simulation model and load line captured for class-B biased at less than threshold values. (b) The Class-B PA using Ideal discrete components (Analog Library) across M1 (65-nm RF-nMOS library)

The drain current generated by the ideal components is also referred as the current generated by SDD. The gate to source voltages for both amplifiers are assumed to be very less than the threshold values. Next section will cover the results of SDD without parasitic effects and ignoring the short channel-length effects. This basic model as seen in Figure 3.4(a) initially shows the targeted ULP consequences. Additionally, it is noted that lowering the parameter current scale's value lowers the saturation current of the transconductance characteristic. You may get a range of knee qualities, from excellent to very "soft," by setting the continuous drain current. The only thing left to do is to manage the critical variables in the equations to get the required device properties for simulations using the real parameters provided by the analogue CAD design tool. These equations are already established for the input-output impedances, drain to source voltages, and output power dissipation. The model will be created in the next part using ideal components from the analogue library of the CAD tool, especially to depict the knee-voltage and transconductance behaviour of the DPA device.

3.3.3 Analysis of Simulation Results for the Classic DPA using Ideal Components

The classic DPA has been simulated without considering channel length and parasitic effects, prevailing the ideal conditions. Figure 3.5 shows the similar architecture for main and peaking amplifier models using the CAD analogue library ideal components. The purpose of this schematic is to exploit the behaviour for class-B and class-C models using the load line analysis discussed in previous section. Both M1 and M2 are biased as common source in medium inversion regions to reduce sufficient amount of DC power. L1||C1 and L3||C3 makes up the oscillator for maximum magnification of current at assigned frequency of 2.4 GHz narrowband signal straight to the input stage, unlike the tradition of using as load impedance at the output of both the main and the peaking PAs. C_2, C_4, and C_{L1}, C_{L2} acts as a DC block at input and output of both amplifiers respectively while L2 and L4 keeps the DC level equal to V_{DD}. An input source (port), labelled as P_{in}, shows the RF(Input) power supplied to DPA. Each RF amplifier has a $Z_0/2$ impedance. A load at power combiner reduced this to Z_0. In order to make it more lossless design, and to avoid unwanted frequencies at the load except to the 40 MHz band, a pi-filter has been adopted at output of peaking amplifier. The pi-filter acts as a lowpass which eventually separate the harmonic effect the load. This pi-filter also fulfils the equivalent impedance provided by the $\lambda/4$ transmission line at the load of peaking amplifier. It is made up of two capacitors, C6 and C7, which are connected to ground by a series inductor L5, as shown in Figure 3.5. This low pass filter provides high impedance at 2.4 GHz high frequency since it is a low pass filter. In order to prevent undesired high frequencies, it is often employed in transmission lines. The classic DPA with ideal components showed a very good result of 1.9mW DC power consumption, 33% Peak PAE, with the operational band of 2.4 GHz, 5.2 dBm P1-dB compression point, 16.14 dB of gain, and a very low value of -17 dB input-insertion loss. Without doubt that these findings are of no worth unless simulated on real environments, with pre and post layout simulations. But it has led us to a state of reliance to build the similar schematic structure on the basis of classic DPA design.

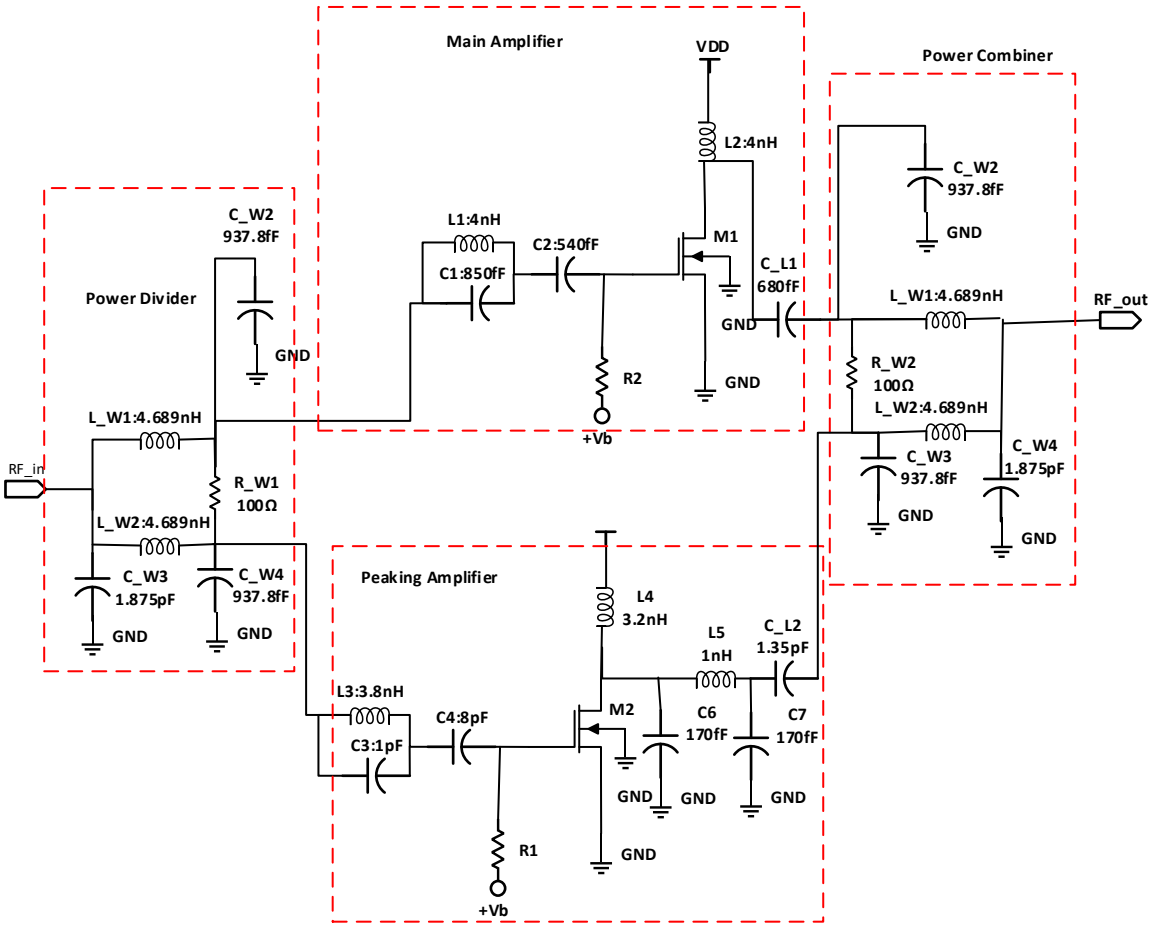


Figure 3.5: The DPA architecture using ideal non-linear analogue library components ignoring the parasitic and channel length modulation effects

The ideal architecture shows a three stage and two-way DPA with ideal readings of efficiency, gain and power consumption. This is a multiway technique where peaking amplifier is connected in line to the main amplifier to get the advantage of maximized OBO. The DPA ideal design implies impedance matching using CAD tool's Analog Design Environment (ADE) which incorporates most optimized nonlinear values, help in getting state-of-the-art results including input return loss, gain, 1-dB compression point, output power and DC power consumption. The similar procedures will be the part of real library designed schematic. Perfect matching of Z_0 is the secret sauce behind these achievements, which add flavours of efficiency at the load of DPA. Figure 3.6 shows the impedance and admittance profiles for both the amplifiers. Examining from the source path

route to determine the input impedance of the main and peaking amplifiers PA are expressed in equations 3.5 and 3.6 as:

$$Z_{in1} = \frac{1}{jwC_{gs(M1)}} + Z_{C2} + Z_{L1} \parallel Z_{C1} \tag{3.5}$$

$$Z_{in2} = \frac{1}{jwC_{gs(M2)}} + Z_{C4} + Z_{C3} \parallel Z_{L3} \tag{3.6}$$

Looking through the output impedances of main and peaking PAs give is expressed in equation 3.7 and 3.8 as:

$$Z_{out1} = Z_{C_{L1}} \parallel Z_{L2} \parallel r_{01} \tag{3.7}$$

$$Z_{out2} = Z_{L4} \parallel Z_{C_{L2}} \parallel r_{02} \parallel (Z_{C6} + Z_{C7} + Z_{L5}) \tag{3.8}$$

where C_{L_1} and C_{L_2} represent the capacitances at both the loads; i.e., the load at the main and the load at the peaking PAs. r_{01} and r_{02} are the drain-to-source resistances of the MOS observed in both PAs. Each overall impedances Z_{Main} and $Z_{Peaking}$ are the functions of input voltage v_{in} (normalized) i.e.:

$$Z_{Main} = \begin{cases} 2R_{opt} & 0 < v_{in} < 0.5 \\ \dfrac{R_{opt}}{v_{in}} & 0.5 < v_{in} < 1 \end{cases} \tag{3.9}$$

$$Z_{Peaking} = \begin{cases} \infty & 0 < v_{in} < 0.5 \\ \dfrac{1}{2}\dfrac{R_{opt}}{v_{in} - 0.5} & 0.5 < v_{in} < 1 \end{cases} \tag{3.10}$$

It is clear that the impedance of main amplifier precisely follows the necessary profile after the breakpoint as illustrated in literature review of Doherty PA.

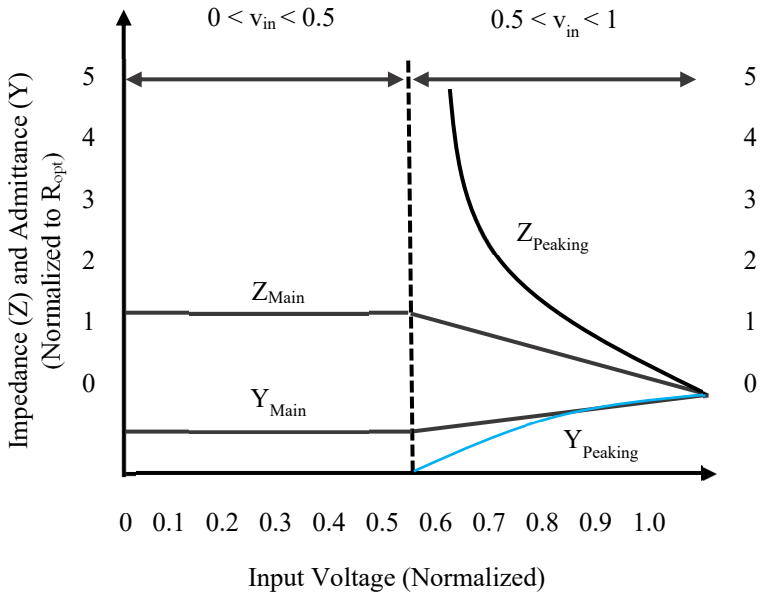


Figure 3.6: Impedance and admittance trend for both the main and peaking amplifiers with respect to the input voltage (normalized)

3.4 The DPA Design, Simulation and Optimization in 65-nm CMOS Technology

The proposed DPA maintains a high degree of power efficiency while being able to handle signals with a greater PAPR. To maximize the amount of power supplied to the load, a perfect matching of 50Ω is required from the RF(Input) stage to the load. Parameters S11 (insertion loss less than -10 dB) and S21 (gain more than +10 dB) reflects the maximum transfer of power from power divider stage to input of both amplifiers. The ideal non-linear components used in DPA architecture of Figure 3.5 were sufficient to achieve the impedance and admittance trend for both the main and the peaking PAs, with respect to the RF(Input). Additionally, the effect of transmission path had nothing to do with the power transfer from input to output stage. Optimizing Figure 3.5 with non-linear 65-nm CMOS technology library components need some additional requirements due to subthreshold operation of M1 and M2. Figure 3.7 is the proposed ULP DPA realized in similar 65-nm CMOS technology. The forthcoming sections will illustrate the impedance matching, power consumption, insertion-loss, gain, output power, power-added efficiency of proposed design [146].

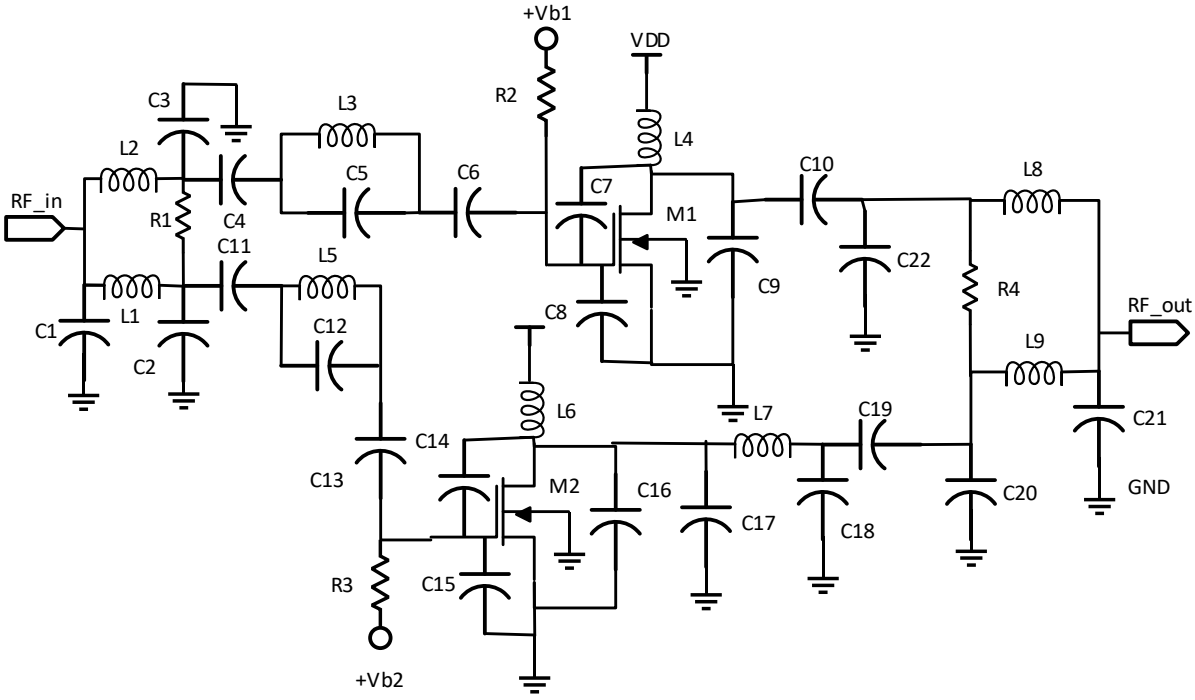


Figure 3.7: Proposed ULP DPA using 65-nm CMOS Technology [146]

3.4.1 Matching input and output impedances and small-signal modelling

Examining from the source path route to determine the input impedance of the main amplifier in Figure 3.7, the equations for Z_{in1}, Z_{in2}, Z_{out1} and Z_{out2} can be optimized as:

$$Z_{in1} = Z_{C4} + \left(Z_{C8} \parallel \left(\frac{1}{jwC_{gs(M1)}} \right) \right) + (Z_{L3} \parallel Z_{C5}) + Z_{C6} \qquad (3.11)$$

As with the peaking amplifier,

$$Z_{in2} = Z_{C11} + (Z_{C15} \parallel \frac{1}{jwC_{gs(M2)}}) + (Z_{L5} \parallel Z_{C12}) + Z_{C13} \qquad (3.12)$$

Calculating the entire output impedance by looking via the main amplifier's output results in:

$$Z_{Out1} = r_{O1} \parallel Z_{C9} \parallel Z_{C10} \parallel Z_{L4} \parallel \left(Z_{C7} \parallel \frac{1}{g_{m1}} \right) \qquad (3.13)$$

Again, for the peaking amplifier

$$Z_{out2} = Z_{L6} \parallel r_{O2} \parallel Z_{C16} \parallel Z_{C19} \parallel (Z_{C17} + Z_{C18} + Z_{L7}) \parallel (\frac{1}{g_{m2}} \parallel Z_{C14}) \qquad (3.14)$$

where Z_{in1} and Z_{in2} are the main amplifier's and peaking amplifier's adjusted input impedances, as measured from the respective sources to the power-divider, respectively.

The main and peaking PA's output impedances, measured and examined from the power-divider routing end to the respective drains, are adjusted Z_{out1} and Z_{out2}, respectively. For perfect matching, the impedances toward PA are measured to 50Ω. To improve the PAE, C4 and C11 are added as fixed interstage capacitances [148] between the power divider and main amplifier & peaking amplifier PAs respectively. Using the measured results of the amplifiers that were developed, the analysed impact of the fixed interstage capacitance is successfully validated in Figure 3.8.

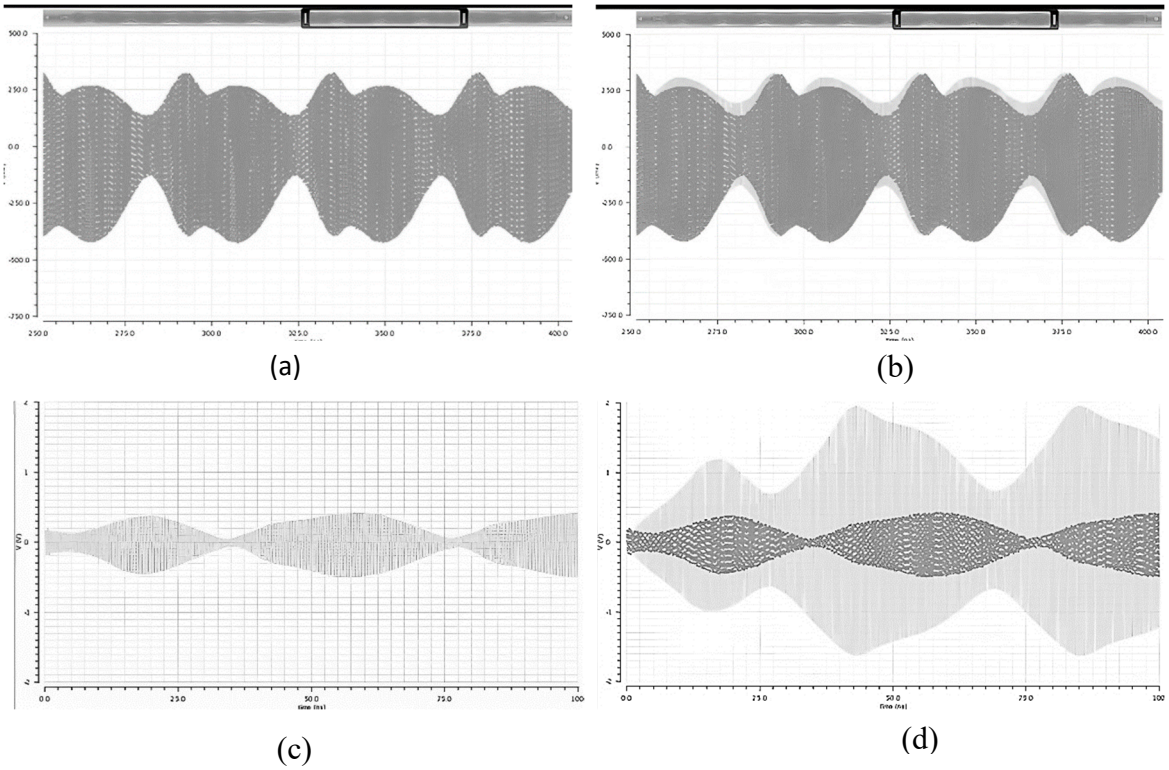
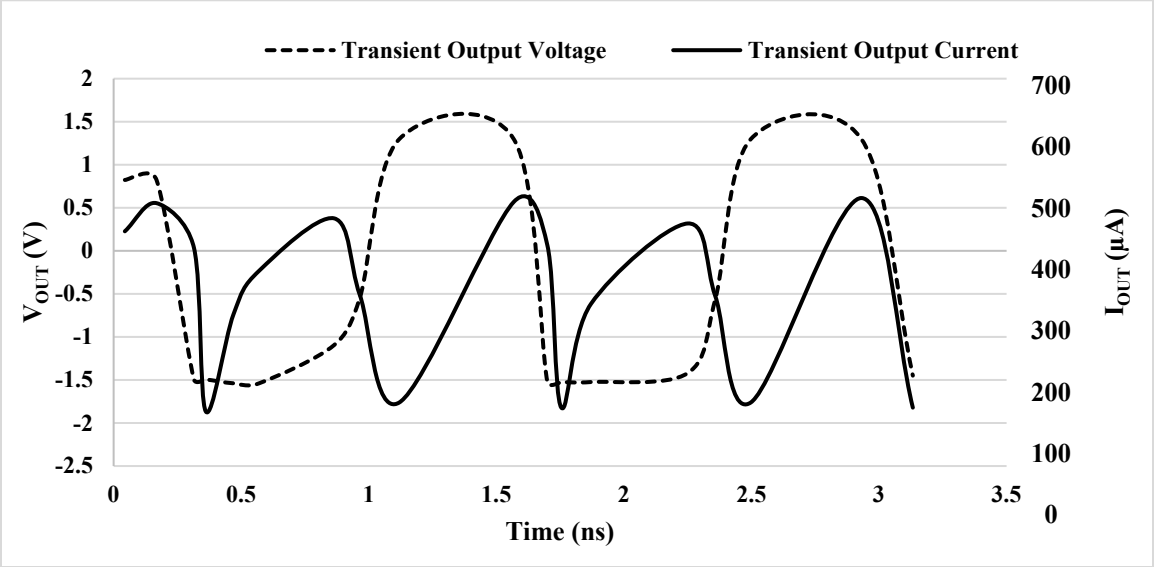
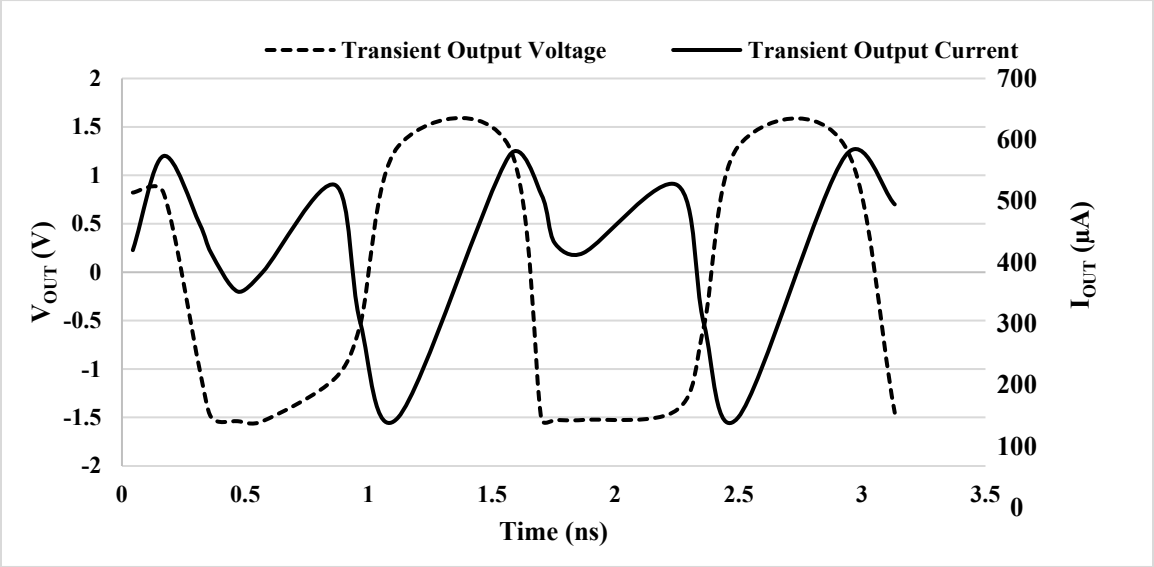


Figure 3.8: The transient state impact (a) before inter-stage capacitance with current magnification and (b) after inter-stage capacitance with current magnification placed between power divider and main amplifier. (c) The before inter-stage state for peaking amplifier and power divider and (d) its effect after the inter-stage capacitance as input approaches -7 dBm [146]



(a) Transient output voltage and current for -20 dBm input



(b) Transient output voltage and current for -7 dBm input

Figure 3.9: Subthreshold operation for main amplifier and peaking amplifier with distinctive (particular) g_m values, operating much lower than the threshold point/ the lower inversion region (a) Transient output voltage and transient output current at -20 dBm input (b) The same as (c) for -7 dBm input [146]

Unlike wideband PAs where only variable or tuned interstage capacitances benefit, the narrowband design for 2.4 GHz frequency (at 40 MHz band) benefits the utmost M1 and M2 biased for subthreshold operation. L5 parallel to C12 and L3 parallel to C5 are positioned to align and adjust the energy constraint at tuned 2.4 GHz fundamental frequency. DC bias is controlled by C6 and C13 (+Vb1 and +Vb2). M1 and M2 exhibit gate-source voltages of 280mV and 290mV respectively, while operating in subthreshold region. In order to adjust the undesirable parasitic capacitances, C7, C8, C9, and C14, C15, C16 (all specifically optimized values) are placed at gate-drain, gate-source & drain-source for M1 and M2. The source impedance levels and extremely slight variations in impedance parameters cause results to differ from those predicted by theories. Contrary to [149], where variable inter-stage capacitance has been seen as a result of wideband, the design has constant inter-stage capacitances with perfect matching of 50Ω.

3.4.2 Subthreshold Operation in Weak Inversion Region

The operation for the input-voltage $V_{GS(M1)}$, as shown in Figure 3.9, is operating at a significantly lower to the threshold. The output seen at the drain of main PA M1 changes as the input changes from -20 dBm to -7 dBm. M1 gate accepts the input, and its drain detect the output. The normalized drain current is related to the transconductance drain current using the g_m/I_d approach, and the power gain is then achieved by further optimizing the results. For M1 biased in class-AB (operating as main amplifier) at subthreshold value of $V_{GS1} = V_{b1} = 280mV$, standard $V_{DD} = 1.2\,V$ and defined $V_{TH} = 450mV$, the performance parameters were seen: $P_{DC1} = 985.1uW$, $g_{m(M1)} = 10.78mS$, $I_{d1} = 547.5uA$, representing $\frac{g_{m(M1)}}{I_{d1}} = 19.74$. M2 biased in class-C (operating as the peaking amplifier) at sub-threshold value of $V_{GS2} = V_{b2} = 290mV$, the following performance parameters were seen: $P_{DC2} = 1.194mW$, $I_{d2} = 663.5uA$, $g_{m(M2)} = 12.64mS$, $\frac{g_{m(M2)}}{I_{d2}} = 19.1$. V_{b1} and V_{b2} (gate to source voltages) are configured at the values shown in Figure 3.9 to significantly cut on the highly nonlinear characteristics. The Taylor expansion [150] represents the circuit design's maximal linearity and to ensure that both amplifiers' suitable

bias voltages are optimized. If I_{ds1} and I_{ds2} represent the non-linear drain-to-source currents, respectively for the main and peaking amplifiers, the following are the equations for expansion:

$$I_{ds1} = gm_{M1}.V_{b1} + \frac{gm_{M1}^2}{2!}V_{b1}^2 + \frac{gm_{M1}^3}{3!}V_{b1}^3 + \cdots \quad (3.15)$$

and

$$I_{ds2} = gm_{M2}.V_{b2} + \frac{gm_{M2}^2}{2!}V_{b2}^2 + \frac{gm_{M2}^3}{3!}V_{b2}^3 + \cdots \quad (3.16)$$

where the factorial powers are the second and third harmonics, respectively.

Equations (3.15) and (3.16) are expressions for third order intermodulation, which is often ignored and seen as being nearly equivalent to zero, is produced by g_m^3.

3.4.3 PAE, Power Consumption, and Small Signal Model for S11 & S21 Validation

As the drain voltage rises, so does the DC power exponentially. When V_{DD} reaches its maximum value of 1.2 volts, Figure 4.1(d) (in chapter 4) indicates the maximum value of 2.1mW as the total DC power usage. Even with low subthreshold values for the DC operating current I_D, both M1 and M2 are operating in subthreshold regions. The following equation theoretically calculate and analyse the total DC power used by M1 and M2 (drain-to-source):

$$P_{dc} = (\mu_n C_{ox})^2 \begin{bmatrix} [\left(\frac{W_1}{L_1}\right)^2 \{(V_{b1} - V_{TH1})V_{out1} - V_{out1}^2\}^2 Z_{L4}] \\ + \left[\left(\frac{W_2}{L_2}\right)^2 \{(V_{b2} - V_{TH2})V_{out2} - V_{out2}^2\}^2 Z_{L6}\right] \end{bmatrix} \quad (3.17)$$

Likewise, no voltage drop is seen across L4 or L6, hence $V_{out1}=V_{out2}=V_{DD}$. For 65-nm technology, the length L1 = L2 = 60nm is the predetermined default value. Using the equation above, one may determine the width to modify the DC power. When the transistor is turned on, the area under the curve will be determined as the ideal width to achieve this

DC power use while retaining the set gate voltage and fixed threshold voltage values. [151]. For our case, W_1/L_1=12µm/60nm and W_2/L_2=18µm/60nm; where n is the number of fingers and m is the width of a finger. The following expressions may be used to estimate each width:

$$W_1 = \int_{V_{off}}^{V_{on}} I_{D1} dV_{out1} \tag{3.18}$$

$$W_2 = \int_{V_{off}}^{V_{on}} I_{D2} dV_{out2} \tag{3.19}$$

$$W_1 = (\mu_n C_{ox})((V_{b1} - V_{TH1}) \int_{V_{off}}^{V_{on}} V_{out1} dV_{out1} - \int_{V_{off}}^{V_{on}} V_{out1}^2 dV_{out1}) \tag{3.20}$$

and

$$W_2 = (\mu_n C_{ox})[(V_{b2} - V_{TH2}) \int_{V_{off}}^{V_{on}} V_{out2} dV_{out2} - \int_{V_{off}}^{V_{on}} V_{out2}^2 dV_{out2}] \tag{3.21}$$

It is worth noting that the width of an nMOS transistor plays a significant role in achieving good PAE at the output. Since the PAE is a measure of the efficiency of a power amplifier in converting DC power to RF output power. The PAE is a key parameter in power amplifier design, as it quantifies the ratio of RF output power to the DC input power. A wider transistor can improve the PAE by reducing the series resistance and enabling higher output power levels. A lower series resistance helps to minimize power losses and maximize power conversion efficiency. Additionally, a wider transistor can reduce the resistive losses due to on-resistance (R_{ds}-on), resulting in improved overall efficiency.

Now it is simple to understand that the PAE of the proposed ULP-PA as $\eta = \frac{P_{out}-P_{in}}{P_{dc}} x100$, where P_{in} and P_{out} are representations for the input and the output powers, respectively. Theoretically, simply due to distinct classes of PA, class-F PAs have the capability to achieve 100% PAE using the aforementioned expression [152]. This is not

achievable for the case of class-B, class-C, or mixed effects of both, and only achievable for switching amplifiers. To accomplish the OBO level at a certain PAE, both biasing voltages at sub-threshold regions are, nevertheless, perfectly matched and tuned. At the 6 dB OBO point, this PAE may be observed. Small signal measurements of class-B and class-C have been performed using small signal analysis. Figure 3.10 shows the small signal model which validates the insertion loss and gain for both classes of PAs.

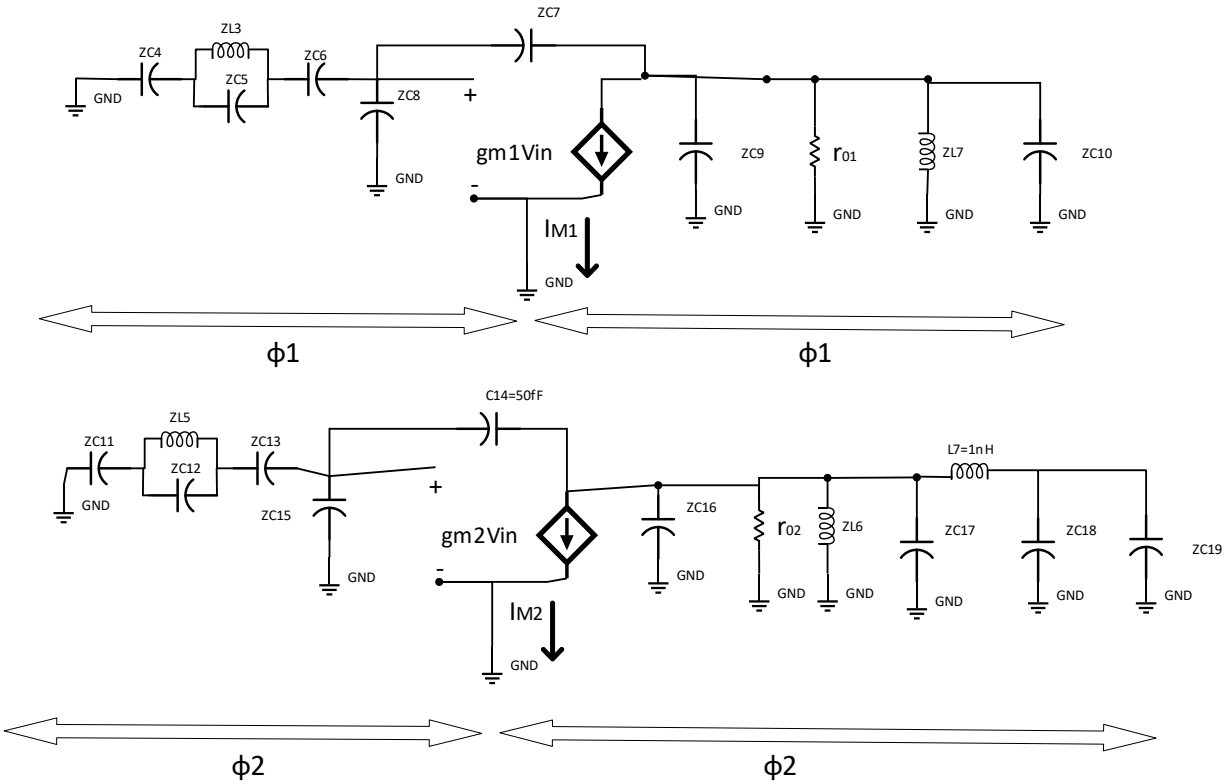


Figure 3.10: Small signal model to measure signal performance of both classes of PA

The DC voltage (which is neglected here) is kept constant at V_{DD}, and the DC current component also increases linearly with the input amplitude. Also, the linear load-line is directly related to the drain-to-source voltage of common source M1, which results in:

$$V_{DS(M1)} = \frac{g_m V_{gs}}{2} Z_{C10} \parallel Z_{C9} \parallel r_{O1} \parallel Z_{L4} \parallel \left({}^{1}/_{gm1} \parallel Z_{C7}\right) \tag{3.22}$$

and

$$V_{DS(M2)} = \frac{g_m V_{gs}}{2} Z_{C19} \parallel (Z_{C17} + Z_{C18} + Z_{L7}) \parallel Z_{L6} \parallel r_{O2} \parallel Z_{C16} \parallel |(^1/_{gm2} \parallel Z_{C14}) \quad (3.23)$$

where both load-impedances are set to Z_{L1} and Z_{L2} respectively, which generally sets both R_{L1} and R_{L2} ($I_D - V_{DS}$ load-line) to:

$$Z_{L1} = Z_{L2} = 2\frac{V_{DD}}{g_m V_{gs}} \quad (3.24)$$

These output voltages will act indifferently at drain-to-source of M1 and M2. The pi-matching network at load of peaking shifts the phase to 180 degrees for V_{out2}, which $\varphi 1 = \varphi 2 = 0^0$ but $\phi 1 = \phi 2 = 180^0$. To ensure linearity it is needed to be guaranteed these conditions: $\gamma_1 = {}^1/_{(1 + \alpha_1 + \alpha_2)}$ and $\gamma_2 = {}^{\gamma_1}/_{1 - \gamma_1}$. Input power of less 10 dB is being reflected to the overall DPA (Wilkinson divider circuit using inter-stage capacitances via the path of lumped parameters to the main and peaking amplifier), which exhibits excellent impedance matching towards the input end. A negative conduction in the reverse circuit is produced by insulation from the gate to the drain for M1 and M2. The gain is increased by a further 10 dB at the output using a similar perfect match.

3.4.4 Effects of Parasitic Component on High Frequencies and Load Pull Simulation

Introducing a higher inductor value at the M1 and M2 drains leads to an increase in parasitic resistance, which in turn results in a decline in efficiency during real simulations. To address this issue, a design package incorporating simulation capabilities was utilized, specifically focusing on the main amplifiers C7, C8, and C9, as well as the peaking amplifiers C14, C15, and C16. Through simulations, it was determined that the ideal inductance value in this context exceeds 4nH, accompanied by extremely small drain-to-source, gate-to-source, and gate-to-drain capacitors for both M1 and M2. The simulation findings reveal an insertion loss of -11.9 dB and a gain of 10.14 dB over a 40 MHz bandwidth ranging from 2.4 GHz to 2.44 GHz.

While discussing parasitic components in this sub-chapter, the focus is primarily on static, passive components. However, it should be noted that certain parasitic effects, such as the nature of input and output capacitance, are dynamic and depend on terminal voltages. Nonetheless, these effects are considered minor or negligible for the purposes of this ideal work. It is important to consider the frequency-dependent behaviour of passive components in high-frequency design. Amplifiers are designed using lumped parameters, which encompass resistors, inductors, and capacitors whose impedance varies with frequency changes. The equations $X_C = {}^{1}/_{2\pi fC}$ and $X_L = 2\pi fL$, employed to compute the reactance for capacitors and inductors respectively, are straightforward.

In addition to the value of an electronic component, its parasitic characteristics are influenced by factors such as size, shape, the use of materials that may deviate from ideal properties, and electromagnetic coupling between closely situated components. It should be noted that the impact of inherent parasitic reactive components on transistor models is less significant when operating at low frequencies.

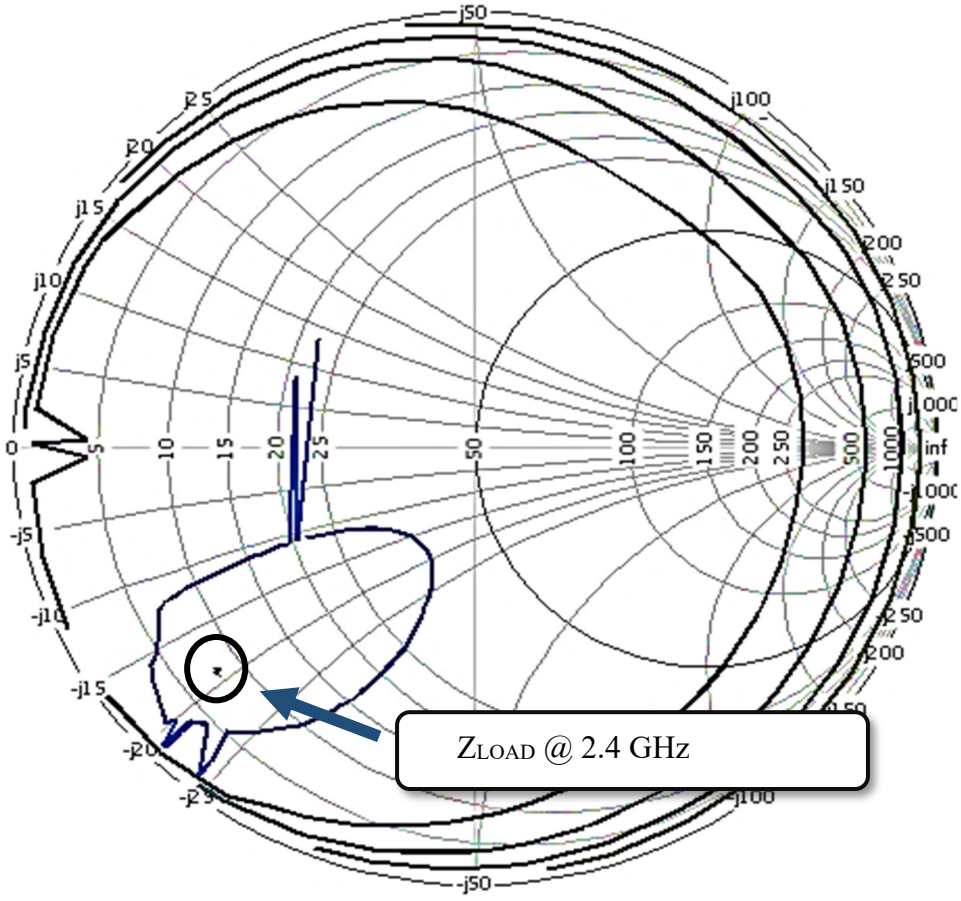


Figure 3.11: The load-pull analysis showing harmonic content and power contours

The maximum output power, gain, or efficiency at a certain load impedance are often determined via load pull simulation and shown on a series of contours in the Smith chart. That impedance will be what an amplifier-designing equipment really sees. Figure 3.11 illustrates how the load pull simulation is carried out in this study, utilizing the built-in Load-pull Instrument in the CAD analogue design environment. While maintaining a steady source power for a single tone, the load-pull instrument's load-pull tuner sweeps the load reflection coefficient. The installation of a de-embedding network for PA device enables for characterization at both the current generator and package plane which is possible to the connection of this instrument to the device. In this context, the terms *current generator* and *package* refer to the intrinsic plane of the transistor, while *package plane behaviour* includes both the transistor and its parasitic elements. The load impedance that is provided to the device may be changed by the load tuner in the load pull. It is based on

a simulation of harmonic balance. The dynamic load-lines and the voltage and current waveforms that produce them for a class-B bias are shown in Figures 3.9 for the two de-embedding methods. It is encouraging to see that both techniques exhibit extremely comparable voltage and current behaviour. The difference can be seen in the off-state portion of the waveforms, where there is clearly greater displacement current since the output capacitance's dynamic nature was not completely de-embedded by the straightforward static embedding method.

The Load-pull Indicator simulates the load using a harmonic balancing simulation controller operating at 2.4 GHz, input power set to -8 dBm, gate bias for class B set to 280 mV, and drain bias set to 1.2V. Figure 3.11 shows that these impedance conditions have been met at the current generator plane and that, because of the presence of parasitic capacitance and inductance at the package plane, a different set of required impedances is required there. It is discovered that the fundamental, unnormalized optimal impedance at the current generator plane is 15.7–j20.4Ω, whereas the second and third harmonic impedances are directed at 0 ohms. The second and third harmonic impedances are rotated to the capacitive side of the Smith chart, while the equivalent fundamental impedance measured at package plane is greater.

When the operating frequency rises and the transistor deviates from its ideal trans-conductive behaviour, reactive parasitic will start to have an impact. However, designed model for the optimal technology in section 3.2 excludes the occurrence of parasitic effect. It is true that in a practical design, parasitic capacitance and inductance must be addressed at RF frequencies in order to avoid mismatch and stability issues at high frequency. Even if limiting the frequency of operation is a valid and practical approach for enhancing a PA design and, for discovering essential Doherty behaviour. DPA design should start with a default-configured load-pull template inside the CAD analogue tool for load-pull simulation. To determine a device's accurate response to the various load-impedances it can end up facing in a real PA setting, load-pull simulation is crucial. It is significant to note that in this design, the intrinsic current generator plane reference and the complete de-embedding of parasitic effects are made possible by the load-pull template. The load-pull simulation is shown in Figure 3.11.

A class-B biased device is used for the individual main PA design, which is followed by a class-C biased PA with a comparable individual peaking amplifier design. Later, a power combiner model and load-modulation were used to improve the combined output. The maximum efficiency, power or gain at a certain impedance at the load are often determined via load pull simulation and shown on a series of contours in the smith chart. That impedance will be what an amplifier-designing equipment really sees. As illustrated, the load pull simulation in this study was carried out utilizing the built-in Load-pull Instrument in the ADE. The load-pull tuner of the load-pull instrument sweeps the load reflection coefficient while keeping a constant source power for a single tone. Due to the connection of this tool to the device, the installation of a de-embedding network for this device allows for characterization at both the current generator and package plane. In this ULP simulation, the load-pull instrument employs a 2.4 GHz harmonic balancing simulation controller with input power set to -8 dBm and gate bias set to 280 mV for class B PA.

A PA can deliver maximum power to its load if it's masked now, we run load-pull simulation to see if the power is maximum in CAD simulation tool, we run periodic steady state analysis to see this load for simulation and after the simulation we can see a set of constant power contours which suggest the maximum power and the optimum load that is necessary to get that power. Figure 3.11 shows the constant power contours on each line where the output power remains constant. This is the optimum load impedance and with this load impedance, maximum output power is received.

3.4.5 Layout of Proposed ULP CMOS RF DPA

The design flow's last simulation phase was transforming the schematic design into a layout. The analytical process is quickly entered using ADE-L, and simulations are conducted. The chip layout features a 0.29 mm^2 active area. The power-rails are used instead of the pads and the pad-effect is included. The ADE-L tier capabilities are expanded by ADE-XL, which offers multiple test support, analysis across sweeps and corners, direct access to all findings, and the ability to generate comparison sheets and datasheets as necessary.

Firstly, the layout editor tool was launched to begin the design process. A new layout cell was created to contain the inductor layout components. The layer stack was defined, selecting suitable metal layers for the inductor windings and determining their spacing and thickness. The drawing and editing tools within the layout editor were utilized to create the desired inductor shape, including the metal traces or coils. Vias and contacts were placed to establish connections between different metal layers and between metal and active device layers. Additionally, appropriate dummy structures and fill patterns were incorporated to optimize the layout for manufacturability and minimize parasitic effects. Design rule checks were performed to ensure compliance with fabrication process guidelines. Layout parasitics, such as capacitance and resistance, were extracted for accurate circuit simulations and analysis. Finally, the completed inductor layout was verified through techniques such as layout versus schematic checks to ensure consistency with the schematic design. The layout design of capacitors began by creating a new layout cell specifically for the capacitor layout components. The appropriate layers for the capacitor plates and interconnects were defined in the layer stack. Drawing and editing tools were utilized to create the desired capacitor structure, considering factors such as size, shape, and spacing. Vias and contacts were added to establish connections between different layers and to integrate the capacitors into the overall circuit layout. Like inductor layout, dummy structures and fill patterns were incorporated to optimize manufacturability and reduce parasitic effects. Design rule checks were performed to ensure adherence to process guidelines. Parasitic extraction was carried out to accurately model the capacitance and resistance of the layout for subsequent circuit simulations and analysis. Finally, the completed capacitor layout was verified through layout versus schematic checks and other verification techniques to ensure its compliance with the schematic design.

To construct the microstrip lines in the layout design, the CAD tool Analog Design Environment (ADE-XL) was employed. The microstrip lines play a crucial role in the overall performance of the Doherty Power Amplifier. The construction process involved careful consideration of the layer stack and the selection of suitable metal layers for the microstrip traces. Using the layout editor tool within the software, a new layout cell was created specifically for the microstrip lines. The layer stack was defined, taking into account the requirements for impedance control and signal integrity. Appropriate metal

layers were chosen to ensure proper signal propagation and minimize losses. The Design Rule Check (DRC) of 0.47 for TSMC 65-nm CMOS technology was kept in mind before placing lines. During the construction process, vias and contacts were strategically placed to establish connections between different metal layers and between the microstrip lines and active device layers. This facilitated the integration of the microstrip lines into the overall circuit layout and ensured proper signal flow. A very few orthogonal lines are visible on layout. However, the 45-degree lines and bend curves are largely preferred.

The most effective task-based environment in the market for simulating and assessing fully customized, analogue, and RF IC designs is called “analogue design environment” in general. When creating the layout, many things are taken into account. Grounding structures between the two input routes are crucial since the design has two distinct inputs for both types of PA, making effective isolation crucial to avoid mixed signals. allowing adequate room for the placement of the wires needed to link the power supply's biasing supply. To assure the proper dimension size and performance, the layout simulation includes a physical representation of the actual component. The final layout design, which was manually produced from the initial schematic and taken into account, is shown in Figure 3.12. To make this design tidy and to make placing the components during manufacturing easier, some rearrangement is done. The layout has been designed without the Sonnet plug-in as no EM simulation is required.

In conclusion, the layout diagram is a crucial phase in the design flow, transforming the schematic design into a physical representation of the IC. The ADE-L and ADE-XL tools played a significant role in conducting simulations and analysis, allowing for thorough testing and optimization of the design. Careful consideration was given to grounding structures, ensuring effective isolation between the two input routes to avoid signal interference. Adequate space was allocated for the placement of wires and power supply biasing. The physical representation in the layout simulation provided confidence in the dimensions and performance of the component. The final layout design, as depicted in Figure 3.12, underwent manual adjustments to enhance manufacturability and component placement. Notably, the layout design did not require EM simulation, hence the omission of the Sonnet plug-in. This comprehensive layout design process ensures the integrity and functionality of the RF PA design [146].

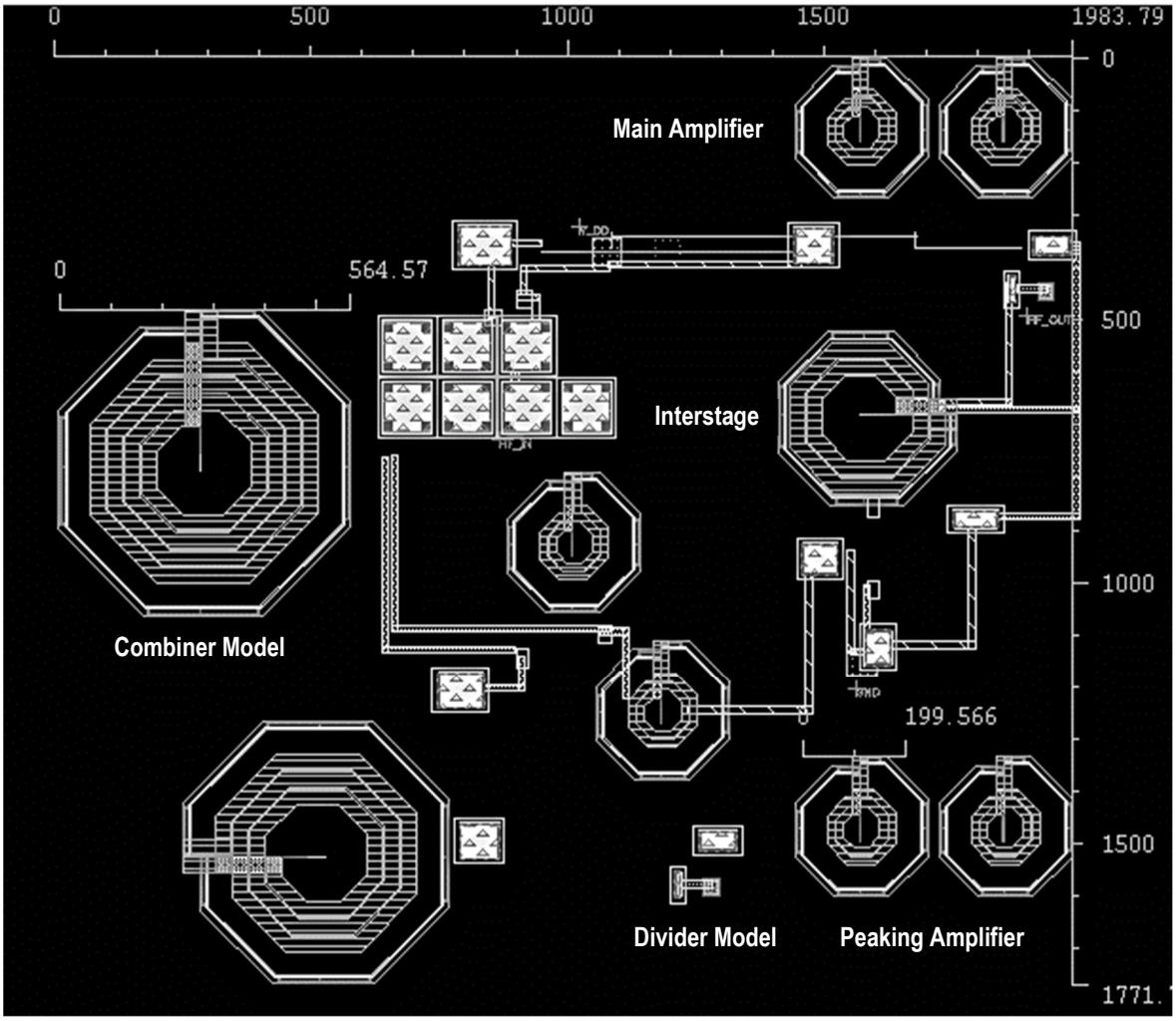


Figure 3.12: Layout of DPA Prototype [146]

3.5 Design and Optimization of Envelope Tracking (ET) Supply Bias with Cascoded Cells Terminated as Class-F ULP-PA for Long-Range and Low Power IEEE 802.11ah WLAN standard

Numerous well-established design methods for Envelope Tracking CMOS Power Amplifiers (ET PAs) that aim to achieve high efficiency have been thoroughly examined in the literature review. The review commences by elucidating the necessary conditions for an ET PA measurement system. Subsequently, the employed ET supply system for conducting the measurements is presented. The design methodology encompasses an

exploration of the capabilities of the ET measurement system, along with a description of the designed essential equipment employed for conducting the tests. The initial step entails restricting any input harmonic component from the input signal to maximize efficiency. This involves the construction of a class-F amplifier with gate-to-drain feedback, aiming to enhance linearity and mitigate harmonic components from the input signal. Two cascode cells terminated as class-F amplifiers are elaborated upon, further contributing to the reduction of harmonic content and improved linearity in the input signal. Additionally, a proposed ET supply biasing approach is discussed, which serves to enhance the efficiency of the class-F PA.

The primary objective of this section is to illustrate the development of a device modelling technique that modifies the input in line with the RF input of a signal within a sub-1 GHz bandwidth. Furthermore, the aim is to reduce system load while maximizing overall system performance. In this chapter, a novel envelope amplifier design based on an ET mechanism is proposed, which exhibits comparable performance. The solution for ET supply bias involves the incorporation of a preamp acting as a linear cascaded amplifier with an envelope detector. Chapter 2 extensively explores the advantages of adopting this linear cascaded stage. The influence of this ET supply is observed in the utilization of two cascode cells terminated as class-F amplifiers within the PA's gate-to-drain feedback system, contributing to improved linearity and reduced harmonic content in the input signal.

3.6 Requirement of ET Measurement System

Implementing a full ET system has a number of challenges, including the need for more accurate biasing and measurement methodologies as well as problems with ET-PA design itself. The ET-PA itself, envelope generation, supply modulation, and the linearization system are a few of the many diverse subsystems that make up an ET system. The ET-PA may be visualized as a three-port device in an ET system with a dynamically adjustable drain bias voltage. Therefore, an ET measurement system must be more complex than a fixed bias PA. Therefore, a measurement system is necessary to satisfy certain criteria, which are covered in more detail in the following subsections.

3.6.1 Comparative Analysis of OFDM BW Ranges for Generation of a Modulated Signal

The process of producing a modulated RF signal and related baseband ET (dynamic bias) signals based on present and foreseeable wireless waveform standards requires an ET measuring system. Commercial CAD software solutions may be used to produce the modulated RF waveforms in the form of I&Q data utilizing a relatively straightforward method. The required baseband signals may be immediately data from I&Q extracted in the form of a signal for the analogue power input (P_{in}), with a 6 dBm overall gain, which is the total gain of all cascaded devices connected before the designed PA. In order to achieve this, 802.11ah transmits an unchangeable innovative communication in the sub-1 GHz ISM band. As mentioned in chapter 2, literature review, this innovation relies on OFDM and offers a variety of bandwidth ranges (1 MHz, 2 MHz, 4 MHz, 8 MHz, and 16 MHz [66]) for data transmissions as well as flexibility in coding and modulation. For carriers operating at 915 MHz, the typical specified bandwidth is at 1 MHz or 2 MHz, and offers greater data-speeds. Signals may be transported further away with a smaller bandwidth. With an output power of 20 dBm, the technology can handle up to 26 channels [67], with the PA supporting a power output of 14 dBm. A 2 MHz channel has an FFT of 64, 56 OFDM subcarriers, 4 pilot-tone carriers, 52 data carriers, and 31.25 kHz for the carrier spacing (2 MHz/64), in addition to the 2 MHz channel (32 seconds). Each of these subcarriers may be implemented using a BPSK, QPSK, 16-QAM, 64-QAM, or 256-QAM subcarriers. There is a 1.78 MHz use of bandwidth included in the 2 MHz total bandwidth. A 4 or 8 microsecond guard interval is included in the 36 or 40 microsecond total symbol duration [68].

Advanced waveforms, like as OFDM, present issues since they allow for high data-rate transmissions even when there are several signal channels between the receiver and the transmitter. As seen in Figure 3.13(a), the transmission employs modulation techniques including Quadrature Amplitude Modulation (QAM) and several carriers, close together. It is important to maintain the amplitude component of the modulation present in these waveforms. The peak handling capacity of the PA must prevent distortion in order to do this. This lowers the average power level that the amplifier can handle since the signal must fall inside the linear domain of the amplifier.

3.6.2 Measurement of Efficiency of PA

To keep up with the need for high-speed data rates, modern wireless communication technologies have been growing quickly. As a consequence, modulation has improved, resulting in a wider bandwidth and higher PAPR. PAs, among other systems, are now required to fulfil high linearity requirements as a consequence. Complex signals with advanced schemes like OFDM on either side cause PAs to perform much worse. Due to the fact that a PA should be used with a back-off from the peak linear output power level and in addition to the PAPR levels, its efficiency quickly drops. In addition, the PA consumes a lot of power from battery sources; thus, improving the PA's performance throughout the whole system model is crucial. For different communication methods, the PAPR varies. Figure 3.13(b) shows how the PAPR grows dramatically when mobile phone networks transition from the entry-level 3G UMTS to the higher-speed 4G LTE.

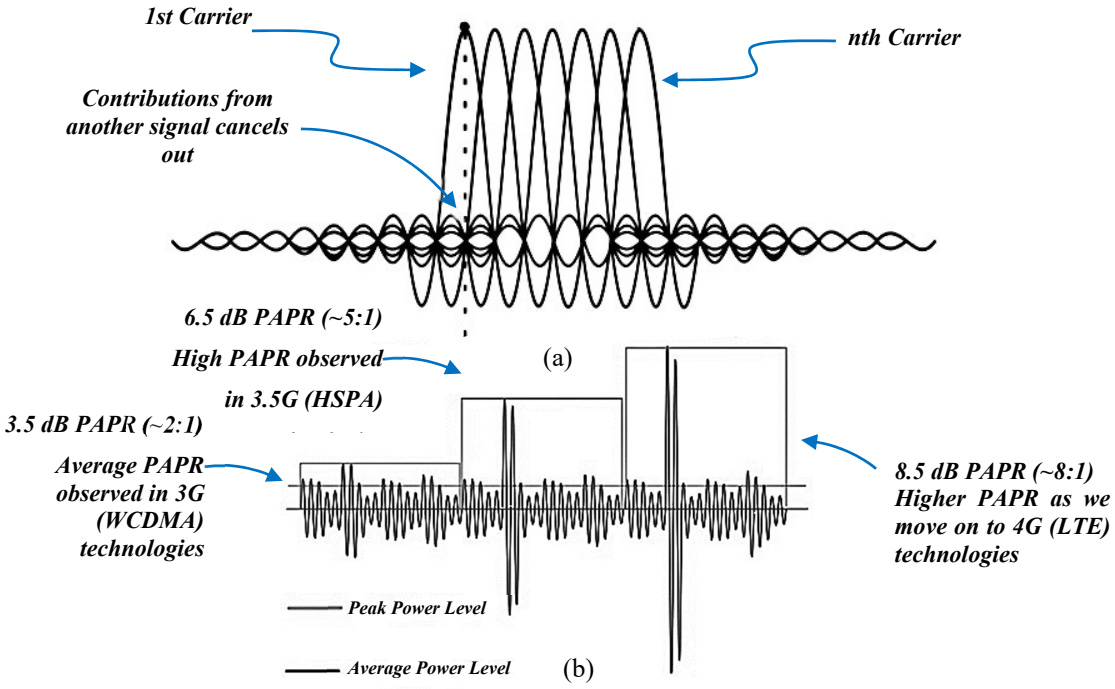


Figure 3.13: (a) In high-speed data rate OFDM waveforms, a quadrature amplitude modulation (QAM) method is used for closely spaced carriers. (b) PAPR rises as technology advances from basic 3G to 4G

The challenge with an increased PAPR waveforms is that the RF PA must be given enough power to handle the peaks while only sometimes making use of this bandwidth since the peaks are present the majority of the time. The amplifier operates at a low efficiency level since this power is lost as heat. As indicated in Figure 3.14, it would be preferable if the amplifier received the appropriate voltage to manage the amplitude of the waveform at any given time. In actuality, it is a technique for an efficient power supply. a condition when the power source is capable of giving the PA precisely what it needs rather than what it demands.

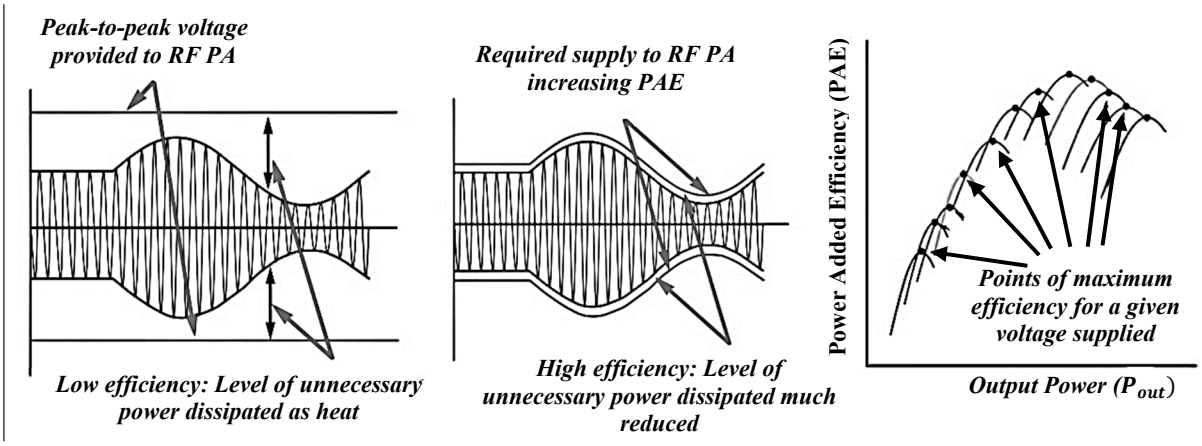


Figure 3.14: Supply provided vs the required supply to RF PA developing PAE

3.7 Fourier Series Analysis of Input Harmonics and Its Impact on PA Design

The trigonometric Fourier series has been used to breakdown the input signal so that the process may be understood. Fourier coefficients are required for it, too. Half of the scale is a real function, while the other half is 0 and will move in the opposite direction. To get the right Fourier coefficients, the signal has been integrated over the non-zero region; the portion of the cosine region depicted here ranges from -2 to +2. The Fourier series equating analysis, which shows that the total of two harmonically dependent sinusoids, provides the solution to this problem. The values for the second, third, and so on harmonics have been entered. For this half-rectified OFDM waveform, analysis shows that all odd harmonics are zero [153]. The unexpected aspect is that the input signal, not the transistor

rectifying the output signal, will provide the harmonics required. As input power rises, the transistor knee voltage falls steadily until it reaches zero. means that the current line crashes towards zero when the transistor load-line reaches the knee region [154] also referred to as the current waveform knee-effect [24]. It has been shown that the odd harmonics produced by a class-F PA are really produced by the transistor's knee area. Additionally, if analysis is exceeded to the next odd harmonic, that is to the fifth harmonic, it is similarly out of phase with the fundamental harmonic, which turns out to be inappropriate for creating square waves. This presents a little difficulty with the Fourier model. The short burst at the current waveform is brought on by non-linear load-impedances producing a non-linearity between the current and voltage. These load-impedances cause harmonic distortion, which has negative impacts on the PA output. Additionally, the current waveform begins to exhibit clipping in the knee region of the transistor as the input power rises further.

Fourier Analysis of I_{pk} as voltage gets < 0:

For a basic class-F half-wave case:

$$(t) = a_o + (a_n \cos(n\pi t) + b_n \sin(n\pi t)) \tag{3.20}$$

$$(t) = \begin{cases} I_{pk} \cos(t)\cos(nt) & -{}^{\pi}/_{2} < t < {}^{\pi}/_{2} \\ 0 & -\pi < t < -{}^{\pi}/_{2}\,;\ {}^{\pi}/_{2} < t < \pi \end{cases} \tag{3.21}$$

$$a_n = \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{-\frac{\pi}{2}} I_{pk} \cos(t)\cos(nt) \qquad provided\ b_n = 0 \tag{3.22}$$

So, the second harmonic:

$$N = 2$$

$$a_n = \left[\frac{I_{pk}}{\pi}\frac{\sin\left(\frac{\pi}{2}\right)}{4} + \frac{\sin(\pi)}{8}\right] - \left[\frac{I_{pk}}{\pi}\frac{\sin\left(-\frac{\pi}{2}\right)}{4} + \frac{\sin(-\pi)}{8}\right] = \frac{I_{pk}}{8\pi} \tag{3.28}$$

And third harmonic:

$$N = 3$$

$$a_n = \left[\frac{I_{pk}}{\pi}\frac{\sin(\pi)}{4} + \frac{\sin(2\pi)}{8}\right] - \left[\frac{I_{pk}}{\pi}\frac{\sin(-\pi)}{4} + \frac{\sin(-2\pi)}{8}\right] = 0 \tag{3.29}$$

for all odd items

Figure 3.15 illustrates how ideally the output current reaches zero when the output voltage waveform deviates from zero because of the knee voltage. The split integration of the current waveform into two halves is the harmonic output. assuming that all values are arbitrary. First from $-\frac{\pi}{2}$ to $-\frac{10\pi}{4}$ (left half) & from $\frac{10\pi}{4}$ to $\frac{\pi}{2}$ (right half), and adding the two components results in:

$$a_n = \frac{1}{\pi}\int_{-\frac{\pi}{2}}^{-(0.1)*\frac{\pi}{2}} I_{pk}\cos(t)\cos(nt) + \frac{1}{\pi}\int_{(0.1)*\frac{\pi}{2}}^{\frac{\pi}{2}} I_{pk}\cos(t)\cos(nt) \tag{3.30}$$

Any harmonics turn negative and non-zero:

$$a_3 = -\frac{I_{pk}}{\pi} * 0.3 \; and \; a_5 = -\frac{I_{pk}}{\pi} * 0.28 \tag{3.31}$$

where the negative sign denotes a 180-degree relative phase. The input signal is what creates the odd harmonics. As seen in Figure 3.15, all odd harmonics for this waveform are out of phase. Therefore, it is difficult to design a higher order square current waveform to increase power dissipation and amplifier efficiency.

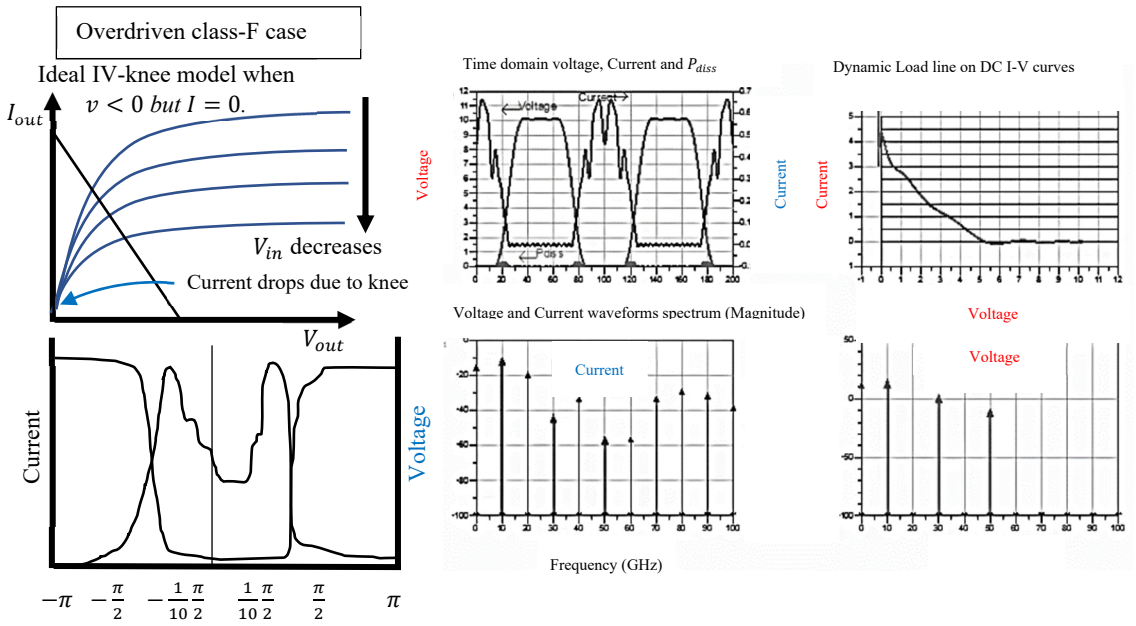


Figure 3.15: The split integration analysis of two waveforms due to transistor's knee-region. I_{out} crashes to zero, as V_{out} goes below zero.

The third harmonic sort of shoots up and drags the centre of the sinusoid away from zero as the voltage waveform near zero, which results in a lesser infringement on the knee area. The integration limits have been modified for an assumption, and they may be solved independently for the three current sections by summing the results together, as shown in Figure 3.15. Most significantly, the current waveform has been modified to produce a perfect square wave by adjusting the fifth and subsequent harmonics, which increases the overall power efficiency of CMOS PA. It is possible to control the transistor's knee region to produce a square voltage waveform and a clipped sinusoidal current waveform, which together make up the basic components of class-F PA operation.

If the coefficients of a time-varying trigonometric polynomial are used to represent the in-phase and quadrature components of the intrinsic device-plane voltage and current, then where is the harmonic order:

$$V_\theta = V_{DC} + \sum_{n=0}^{N-1} V_{nr} \cos(n\theta) + V_{nq} \sin(n\theta) \tag{3.32}$$

$$I_\theta = I_{DC} + \sum_{n=0}^{N-1} I_{nr} \cos(n\theta) + I_{nq} \sin(n\theta) \tag{3.33}$$

Normalizing the coefficients to the DC term and defining in terms of the basic real voltage and current are helpful.

$$v_{nr} = \frac{V_{nr}}{V_{DC}} \; and \; i_{nr} = \frac{i_{nr}}{I_{DC}} \tag{3.34}$$

$$v_{nq} = \frac{V_{nq}}{V_{DC}} \; and \; i_{nq} = \frac{i_{nq}}{I_{DC}} \tag{3.35}$$

The algorithm presupposes a constant ideal current waveform that is "universal" across all device sizes and frequencies and is selected for its high to maximize. A half-wave rectified sinusoid is a popular option since it may be used without sophisticated driving hardware. In order to optimize the fundamental to DC real power ratio, the voltage and current waveforms are combined with a similarly high voltage waveform. However, the voltage waveform must be subjected to restrictions in order to produce a result that is practically usable. In order to reduce the number of harmonics that the matching network must control, the harmonic content must first be suitable low. It is typically assumed that extremely high-order harmonics will experience impedances that are almost short circuited, because of the parasitic drain-source capacitance of the device.

Second, the waveform has to adhere to the physics of the instrument (see Figure 3.15, the transistor knee-region). Any effort to obtain a negative value is impossible since doing so would result in a severe interaction with the transistor's knee/ohmic region that would clip the current waveform and cause significant non-linearization problems. The clipping will ultimately limit if it is quite strong. The prevention of such non-linear excursions of voltage into the knee area is a key component of the clipping contour design process. Additionally, the voltage peaks must have an acceptable low peak value so as not to cause the device to fail. This is done on the assumption that the current generator is an ideal device. In order to examine the intrinsic or current generator (I_{gen}) impedances, parasitic are neglected and an effort is made to de-embed these parasitic on a genuine device.

These waveforms convert to a single set of matched impedances in the impedance domain. The next step is for the PA designer to create a matching network that satisfies these harmonic impedance requirements. This need is a major source of annoyance for the PA designer, who is given matching components whose impedances vary greatly with frequency. The operational bandwidth of these high-efficiency modes is inherently constrained as a result. Using filters with several poles to enhance the bandwidth is one way to address this issue. As each extra pole increases the matching circuit loss and causes a drop in both power and, this is seldom practical in reality. In order to integrate the movement of the circuit impedances in the ideal matching impedance domain, continuous modes alter the voltage waveform and change the harmonic components. The equation for the Class B/J voltage waveform is illustrated in (4.12). A linear "design space" is the outcome, as illustrated in Smith cart of previous design.

$$V_\theta = [1 - \cos(\theta)][1 + \beta \sin(\theta)] \tag{3.36}$$

The designer's job has become much easier as the matching network is no longer limited to a single set of different impedances; instead, to the extent that the technology of the device in question can survive the higher peak voltages, a degree of freedom has been added that allows for the matching network to shift with frequency. These high peak voltage modes are appropriate for new high voltage breakdown device technologies like gallium-nitride (GaN), but the continuum has been shown to be as true for more established GaAs and silicon technologies. In order to reduce loss and expense, this flexibility may be exploited to reduce the number of poles in matched networks, or the network can aim a wider bandwidth for the same number of poles. This is crucial since even systems with substantial bandwidth suffer from performance degradation caused by every extra filter pole. The continuous class-F voltage waveform family, which generates the same trade-off between a larger matching trajectory on the Smith chart and greater peak voltages, exhibits the same characteristics.

3.8 The Proposed Class-F ULP-PA using ET Supply Bias in 65-nm CMOS Technology

To maximize performance in terms of DC power consumption and efficiency, a number of class-F design topologies have been suggested. The device parasitic may be used as part of the circuit topology's harmonic termination network, which is one approach. In order to correctly terminate all of the harmonics, [155] entail providing harmonic impedances to the device from the outside. In order to realize and suppress harmonics at lower frequencies, Hayati presented unique ways such using an asymmetric lowpass filter [156] and biasing a harmonic control network using LPF [157]. For lower frequencies and at the fundamental value, a simple lowpass matching network at a CMOS PA's drain output cancels out the reactive component of the load. However, the parallel parasitic capacitance resonates with the external short to produce a second harmonic short, and the series parasitic inductance is incorporated into that external short to produce a high impedance termination for the third harmonic. This method is used by [158] at Ku-Band to show a class-F mode in a PHEMT procedure. It turns out that at higher frequencies, the LC values from this network are extremely realizable. The inductance falls off as the frequency rises. However, the relative inductance values rise for a sub-1 GHz CMOS PA, increasing the chip's total size and price. The circuit designers must design and build with a very big footprint, on the order of $125um^2$ [159], to get a 5nH inductance value that is reasonable.

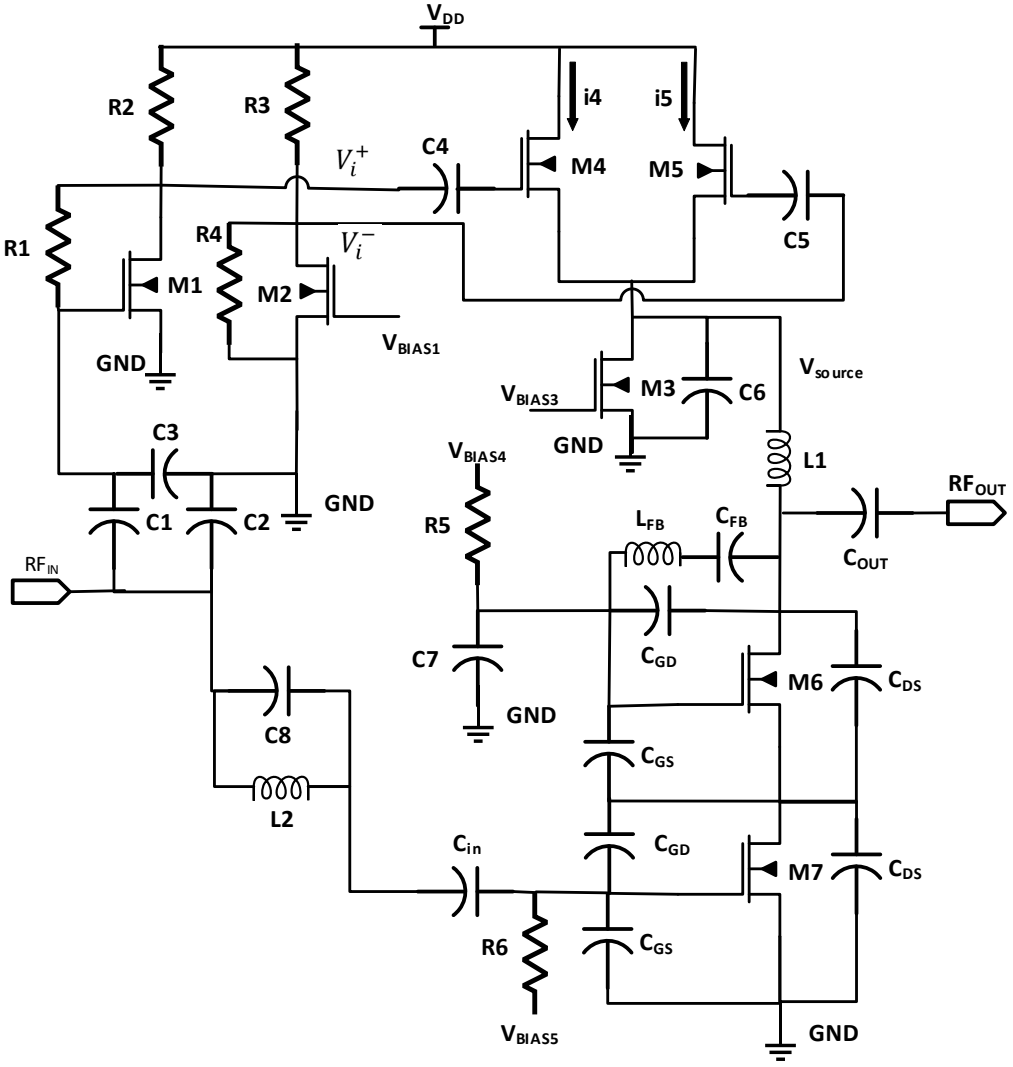


Figure 3.16: Simplified schematic for ULP RF PA class-F cascode terminated as gate-to-drain feedback PA using proposed ET supply architecture in 65-nm CMOS technology

3.8.1 Pre-Amplifier Stage with Envelope Detection

The simplified schematic design of the proposed PA has been depicted in Figure 3.16. The preamplifier, which uses M1 and M2 as the corresponding CS and CG, has enhanced the high frequency modulated RF(Input) signal. High bandwidth uplift and transconductance at drain are features of M2. The CG based M2's low output impedance is

an excellent fit for the next stage. CG has a lower output impedance than the CS-based M1, in comparison. The 50Ω input matching criterion remains a difficulty in amplifier design for maximum signal transmission with minimal losses in the case of sub-1 GHz frequency band. Inductor compensation for C3 is achieved via narrowband input matching using C1||C2. The output swing of the voltage gain (voltage conversion) output of the preamp, which has a sufficient shift to frequency modulated signal voltage ($V_{rf(in)}$), is offset by around ~45% [160].

The following equations are used to coordinate the sizes of M1 and M2 in order to create a gain balance between the preamp's differential outputs and the gate bias voltage variations:

$$g_{m(M2)}/g_{m(M1)} = R_2/(R_1 + R_2) \tag{3.37}$$

$$g_{m(M1)} = 1/(R_1 - R_3) \tag{3.38}$$

where R_1 serves as a feedback resistor for M1, which results in a self-bias and a saturation-level negative feedback output. As illustrated in Figure 3.17, below pinch-off condition is optimum for sufficient DC power consumption for sub-threshold operation. By modifying the overdriven voltage relative to the voltage supplied, M3 is made to function optimally as a current source, finally operating as a higher load resistance with an extended channel length to control the branch current. The following equations may be used to represent the output for M1 and M2:

$$V_p = V_{out(M1)} = R_1/(R_1 + R_2)\, V_{DD} + R_2/(R_1 + R_2)\, V_{TH} \tag{3.39}$$

If $V_{GS} < V_{TH}$ then

$$V_{out} = R_1/(R_1 + R_2)\, V_{DD} + R_2/(R_1 + R_2)\, V_{in} \tag{3.40}$$

$$V_n = V_{out(M2)} = V_{DD}R_4 + R_D(V_{BIAS1} - V_{TH})/R_3 + R_4 \tag{3.41}$$

where adding R_3 and R_4 justifies the inverse relationship to $V_{out(M2)}$.

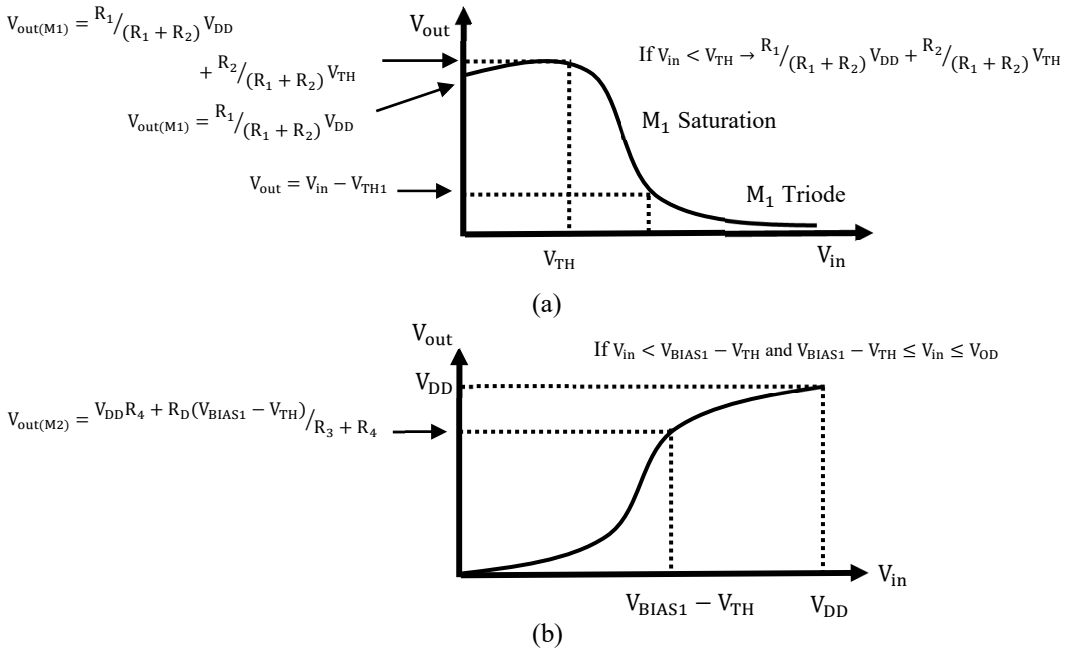


Figure 3.17: Behaviour of (a) M1 for the case of $V_{in} \leq V_{TH}$ and $V_{in} > V_{TH}$ and (b) M2 for the case of $V_{in} < V_{BIAS1} - V_{TH}$ and $V_{BIAS1} - V_{TH} \leq V_{in} \leq V_{OD}$ [160]

The small signal voltage-gain $A_{V(M1)}$ and $A_{V(M2)}$ can be represented by the following equations:

$$\frac{V_p - V_{in}}{R_1} + g_m V_{in} + \frac{V_p}{r_{01}} + \frac{V_p}{R_2} = 0 \tag{3.42}$$

$$A_{V(M1)} = {V_p}/{V_{in}} = -\frac{g_{m(M1)} - {1}/{R_1}}{{1}/{R_1} + {1}/{R_2} + {1}/{r_{01}}} \tag{3.43}$$

and

$$\frac{V_n - V_{in}}{r_{02}} + \frac{V_n}{R_3} - g_{m(M2)}V_{in} = 0 \tag{3.44}$$

$$A_{V(M2)} = {}^{V_n}/_{V_{in}} = \frac{g_{m(M2)} + {}^{1}/_{r_{02}}}{{}^{1}/_{R_3} + {}^{1}/_{R_4} + {}^{1}/_{r_{02}}} \tag{3.45}$$

Figure 3.16 shows the single-ended ED output design. The Preamp output is differentially coupled to the bias gates of the ED at M4 and M5, while the CD and CS drains respectively offer low and high impedances. Assuming the envelope modulated waveform $V_{rf(in)}$ be expressed as:

$$V_{rf(in)} = V_{rf}\cos(w_{rf(in)}t) \tag{3.46}$$

And $({}^{W}/_{L})_n$ be modified to carry the current in accordance with M3's definition of capacity. According to M4 and M5, the drain current values i_4 and i_5 can be expressed as follows:

$$i_4 = {}^{1}/_{2}\,\mu_n C_{ox}({}^{W}/_{L})_n(V_{GS(M4)} - V_{TH} + V_{rf(in)})^2 \tag{3.47}$$

or

$$i_4 = {}^{1}/_{2}\,\mu_n C_{ox}({}^{W}/_{L})_n\,(V_{OD} + V_{rf(in)} \tag{3.48}$$

Similarly,

$$i_5 = {}^{1}/_{2}\,\mu_n C_{ox}({}^{W}/_{L})_n\,(V_{GS(M5)} - V_{TH} + V_{RF(Input)})^2 \tag{3.49}$$

or

$$i_5 = {}^{1}/_{2}\,\mu_n C_{ox}({}^{W}/_{L})_n\,(V_{OD} + V_{rf(in)})^2 \tag{3.50}$$

And the sum of currents to M3 can be expressed by solving (4.24) and (4.26):

$$\begin{aligned} i_{s(4,5)} &= \mu_n C_{ox}(W/L)_n(V_{OD}^2 + V_{rf(in)}^2 \\ &= \mu_n C_{ox}(W/L)_n.(V_{OD}^2 + \frac{1}{2}V_{rf}(t)^2(1+\cos(2w_{rf(in)}t)) \end{aligned} \tag{3.51}$$

where μ_n, C_{ox}, and V_{OD}, represents the mobility of n-MOS, gate-oxide capacitances per unit area, and overdrive voltages.

This part serves as an illustration of the output voltage equations. Using the exponential transfer that the n-MOS transistor creates while it's running in the weak inversion zone, together with a low-pass filter, the baseband information from the RF carrier is retrieved. The ED circuit does not have a differential output, despite having a differential input. Due to the transfer function's squaring nature [161], output amplitudes for both positive and negative RF(Inputs) are the same. According to a design approach set out in [162], when inputs are provided to the source node, the gate oxide capacitance does not undergo capacitive division. It has been recommended to use two p-MOS in differential arrangement in order for the RF signal which is then down-converted into its baseband. When using the same gate layout, a design problem is presented by the transistor's comparatively small input impedance when looking straight at the source node. When the input impedance is insufficient or too low, the ED may load the pre-amp. The pre-amp's impedance at the output is in the range of a few kilo-ohms. The suggested ED design does not overburden the pre-amp as a consequence. To save chip space and cut costs, the load resistances (passive components) at the differential topology drain have also been eliminated. In order to add more and more devices, modern approaches favour n-MOS active loads, which is not optimal for ULP [163].

3.8.2 ED Conversion Gain Using Source Follower Differential Circuit

The realization of both positive and negative RF(Input) in the same region is indicated by the ED conversion gain. In the subthreshold region, M4 and M5 are biased as a differential pair, serving as a source follower or a general buffer differential circuit. Pre-amp signals V_i^+ & V_i^- are applied to gates M4 and M5, respectively, and the output is

obtained using a combined source. We'll make the simple assumption that the common-mode voltage is zero. The drain current equations (3.50) and (3.52) are revised to reflect the fact that M4 and M5 are operating in the weak inversion region (sub-threshold) as follows:

$$i_{d,M4} = i_4 e^{V_G - V_{TH}/nV_T}\left(e^{-V_S/V_T}.e^{-V_i^+/V_T} - e^{-V_D/V_T}\right) \tag{3.52}$$

$$i_{d,M4} = I_{Q,M4} e^{-V_i^+/V_T} \tag{3.53}$$

$$i_{d,M5} = i_5 e^{V_G - V_{TH}/nV_T}\left(e^{-V_S/V_T}.e^{-V_i^-/V_T} - e^{-V_D/V_T}\right) \tag{3.54}$$

$$i_{d,M5} = I_{Q,M5} e^{-V_i^-/V_T} \tag{3.55}$$

where n is the slope of the transfer function resulting from capacitive division and $I_{Q,M4}$ and $I_{Q,M5}$ are referred to as the quotient currents. Equations (3.54) and (3.56) are exclusively valid for common drain, in contrast to equations (3.55) and (3.57), which are both valid for common drain and common source topologies. Thus, adding the two results yields:

$$i_{d,M3} = I_{Q,M4} e^{-V_i^+/V_T} + I_{Q,M5} e^{-V_i^-/V_T} \tag{3.56}$$

Study [164] used V_{DS}/L to represent the electric field and optimized the quotient. And this quotient current is what is created in a weak inversion. The analysis of the n-MOS power detector that came before it makes the assumption that the detector response was read out as a DC-current, maybe using a transimpedance amplifier similar to the one shown in [165]. The current responsivity (input-output gain) is determined by the detector input power P_{in} and is:

$$I_{v,M3} = I_{d,M3} P_{in} = I_{d,M3} \frac{V_{RF}^2}{R_{in}} \quad (3.57)$$

where R_{in} is referred to as the real component of the RF(Input) impedance of the detector.

Equation (3.58) states that the current responsivity is mostly independent of the gate bias when the device is operated in weak inversion. The maximum short-circuit current responsiveness is attained close to the threshold voltage. With reference to subthreshold gate bias, internal current shunting is what results in the poor roll-off of inversion current. By acting as an ET power source, instead of using current readout mode, the detector circuit might use voltage readout mode, a low-noise transimpedance amplifier is not required to provide a high - energy output voltage. In this case, the channel's current and DC conductance produce the voltage seen at the drain.

Typically, the output capacitor may be incorporated for values up to 100 pF depending on the manufacturing method. In the event of a low to high step, larger value makes it possible to react to current demand more rapidly since it serves as a charge supply. However, the size of this output capacitor has a significant impact on the frequency response and stability. There is a trade-off between the minimum phase margin that can be achieved under stand-by conditions and the value of the output capacitor with the compensation topology used in this circuit. The value of CL has an inverse relationship with the phase margin. The output capacitor has no effect on the phase margin in the event of a severe load scenario. In the operational range, a minimum phase margin of 90 degrees is attained, guaranteeing a steady control even under small load.

3.8.3 Two Cascoded-Cells Terminated as Class-F with Gate to Drain Feedback

M6 and M7 behaves as two cascode cells terminated as class-F with gate-to-drain feedback. For a standard configuration, each transistor consists of a common-gate (CG) with a fixed-bias gate-voltage and a common-source (CS) as a transconductance stage. The CG stage is prevented from entering the triode region at a high output power region by the corresponding RF AC signal to the gate node of CG stage. The parasitic gate-drain capacitance maintains a constant level in this regard, enhancing linearity. The current

combining technique with lowpass filter is utilized to combine both cells. For an optimized amplification of Class-F, in which the voltage and current waveform at a drain node form a square and one-half sinusoidal, whereas load-impedance has been adjusted as an optimum resistance with Z_L (2f) as short circuit and Z_L (3f) as open circuit. When the input power is low, the drain voltage is high enough to keep M6 saturated, fulfilling the requirement that V_{DG7} is larger than V_{TH7}, where V_{TH7} is the M6 turn-on voltage. C_{DG}, C_{DS} and C_{GS} are placed to avoid effect of parasitic capacitances which cause AM/PM distortion and also helps in perfect matching of 50Ω with next stage. These variations in supply causes non-linearity in OFDM RF-input due to supply variations during various stages in PA. L_{FB} and C_{FB} are feedback inductor and capacitor respectively, which reduces insertion losses across the small band of 915 MHz. To verify the superior performance of the proposed technique, a CMOS PA was designed using a commercial 65-nm process. The PA has a 14.3 dBm power gain and a 22 dBm total saturated output power with 37.1% PAE.

A partial output signal is introduced into the gate node of M6 using the proposed gate-drain feedback network, which consists of an inductor L_{FB} and capacitor C_{FB}. As the drain voltage drops, so does the adjusted gate voltage in a proportional manner. As a result, even at high power levels, M6 has the ability to function in a saturation region. In addition to compensating, the ideal value for L_{FB} and C_{FB} is meticulously chosen to reduce insertion loss throughout the feedback path. In this study, 2.3nH and 3.4pF are used and inductor and capacitor values. The impedance observed at the output due to this feedback path is 12.2-30.6jΩ. If an increased gain signal for instance 6 dBm at the input of a transistor that is already biased in the subthreshold region, the transistor will move to the saturation region. This is because the gain signal will increase the V_{GS} above the V_T. When V_{GS} is greater than V_T the transistor will enter the saturation eventually producing adequate drain current. But no impact on voltage even at higher RF input, is observed due to feedback mechanism. Figure 3.18 shows the drain-gate voltage waveform at M6 for various input power levels.

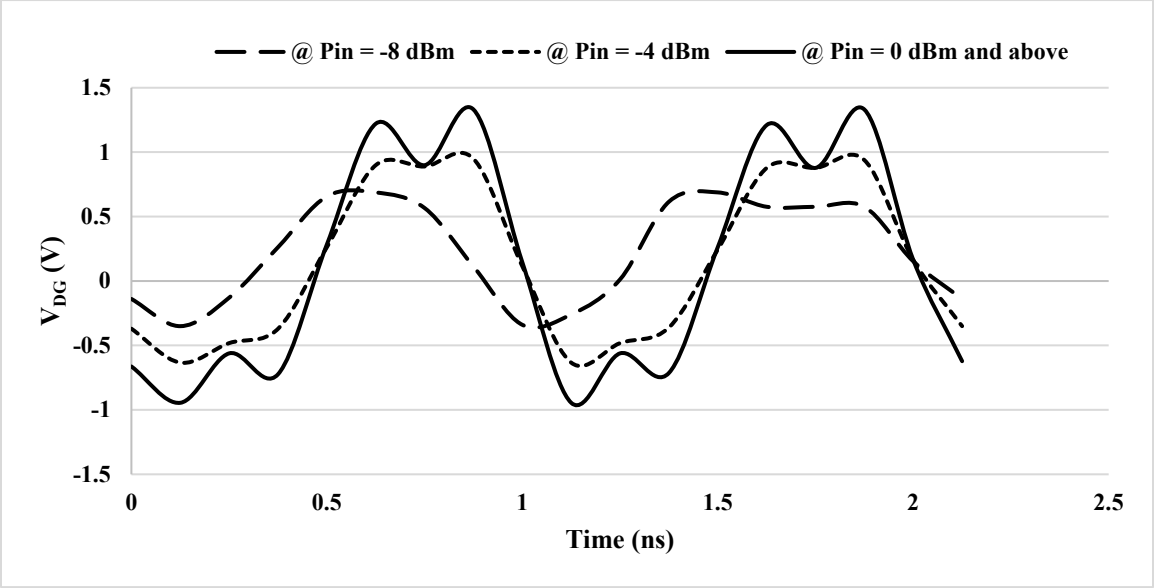


Figure 3.18: Drain-gate voltage waveform at M6 for various levels of Pin

3.8.4 Power Consumption Under Subthreshold Weak Inversion with Proposed Design Parameters

In accordance with the CD design, M2 would normally operate in the saturation region when compared to the subthreshold region. M1 is still in a weak subthreshold inversion. The following observations have been made: $^{W}/_{L}\,(M1) = {}^{W}/_{L}\,(M2) = 12\mu m/60nm$, $^{W}/_{L}\,(M3) = 22\mu m/60nm$, $^{W}/_{L}\,(M4) = {}^{W}/_{L}\,(M5) = 18\mu m/60nm$, $^{W}/_{L}\,(M6) = 12\mu m/60nm$ and $^{W}/_{L}\,(M7) = 14\mu m/60nm$. Also, the dc powers for defined configurations are observed as: $P_{dc(Preamp)} = 0.12mW$, $P_{dc(Differential\ ED)} = 1.29mW$, $P_{dc(Cascoded\ Cells)} = 2.34mW$. The proposed design parameters propose parasitic capacitances between drain-to-source (C_{DS}), drain-to-gate (C_{DG}) and gate-to-source (C_{GS}) are 50fF. The transistor's behaviour and potential for signal distortion are affected by the C_{DG}, which connects the input signal to the gate voltage while the series feedback L_{FB} and C_{FB} as 2.3nH and 3.4pF respectively.

3.8.5 Layout of Proposed CMOS RF ET Supply Bias using Cascoded Feedback class-F PA

As shown in Figure 3.18, the chip layout features a 0.13 mm^2 active area. Only the cascoded feedback class-F design, which evidently takes up the major area. The LC tuning range is 915 to 931 MHz, as measured. For ET supply biasing, the inductor-less design saved up to 88% of chip area [166]. The proposed design offers a very low DC power usage and up to 57% conversion gain, the lack of decoupling capacitors, a low output impedance -all of which are essential for ET supply-biasing, and can precisely follow the modulation envelope at the greatest bandwidth frequency. The last simulation step of the design flow was transforming the schematic design into a layout. The analytical process may be quickly entered using ADE-L, and simulations can be conducted with ease. The ADE-L tier capabilities are expanded by ADE-XL, which offers multiple test support, analysis across sweeps and corners, direct access to all findings, and the ability to generate comparison sheets and datasheets as necessary. The most effective task-based environment in the market for simulating and assessing fully customized, analogue, and RFIC designs is called ADE-L. When creating the layout, many things are taken into account. Grounding structures between the two input routes are crucial since the design has two distinct inputs for both types of PA, making effective isolation crucial to avoid mixed signals. allowing adequate room for the placement of the wires needed to link the power supply's biasing supply. To assure the proper dimension size and performance, the layout simulation includes a physical representation of the actual component. To make this design tidy and to make placing the components during manufacturing easier, some rearrangement is done. The signal is routed on layer M4, somewhere connected to M5 upon requirement. The VDD and GND are routed using M1 layer. The power-rails has been used instead of the pads and the pad-effect is itself included in power rails for the CAD tool layout version. Also, the layout has been designed without the Sonnet plug-in as no EM simulation is required [160].

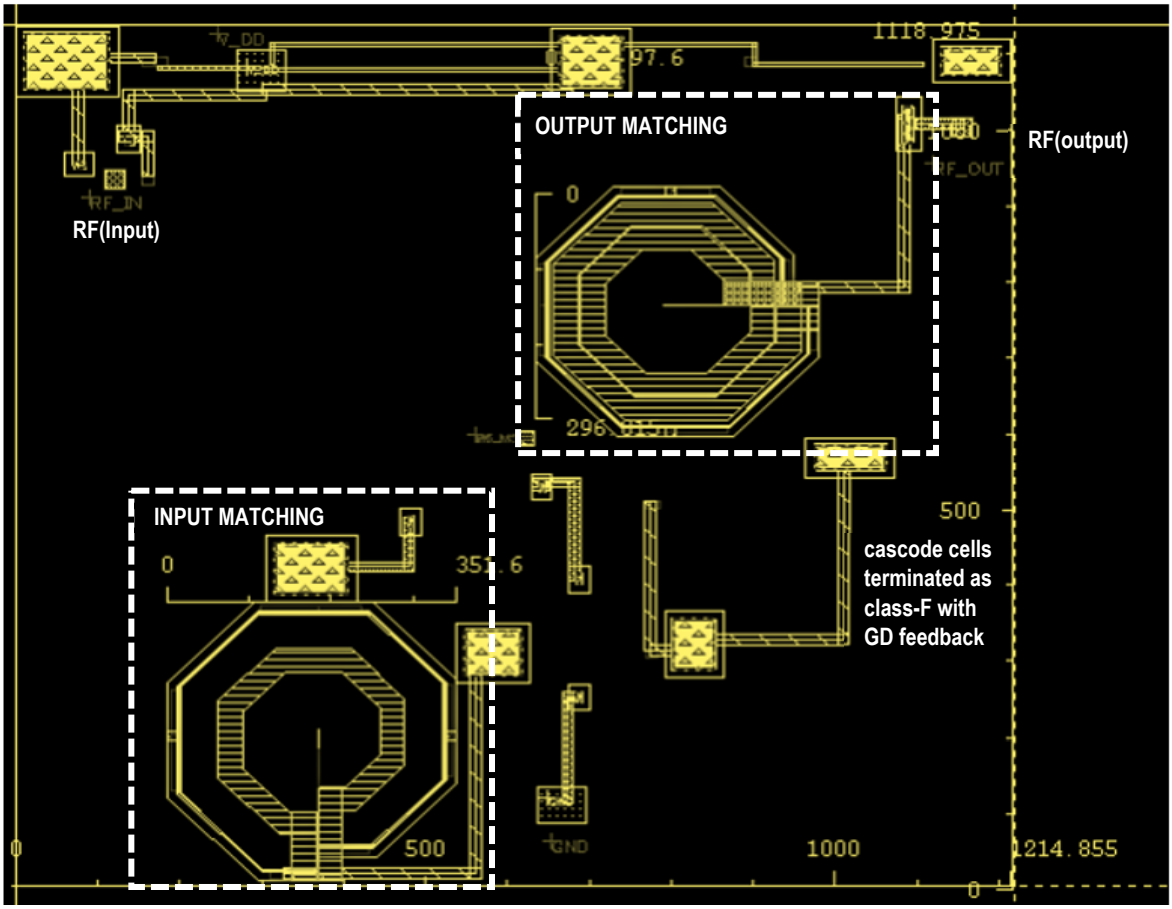


Figure 3.19: Layout of proposed ET Supply bias to cascode cells terminated as class-F with GD feedback ULP-PA in 65-nm CMOS technology [160]

3.8.6 Analysis of load pull for class-F PA

Observe the transistor's load-impedance; it reveals open circuit behaviour for odd harmonics and closed-circuit behaviour for even harmonics. The circuit does not operate as an ideal switch when employing real PA components. As a consequence, harmonics are produced in both open and closed circuits. Now that the transistor circuit has a non-linear model, load pull analysis may be performed. By doing so, you may calculate the highest power output possible given the load-impedance. The power contours in CAD tool offered by 65-nm CMOS technology may be used to get the maximum PAE and the maximum output power via load-pull analysis. Figure 3.20 displays the load-pull and output power

contours. The input impedance still has to be matched to 50 ohms even if the overall in-design impedances seem to be nearly right at the harmonics. In order to return the reactive fundamental impedance to its ideal value of 50 ohms, a simple LC low pass matching network may be created on the Smith chart; however, the insertion of this matching network causes the harmonic traps to shift significantly. The third harmonic is no longer a perfect open, and neither is the second harmonic a perfect short. It is necessary to reoptimize the circuit in order to get the fundamental impedance, and all the harmonic impedances, appropriate. To do this, set up a few components for automated optimization and then add a few simple re-optimization objectives. The optimization yields in a matching network that perfectly meets each of these configurations.

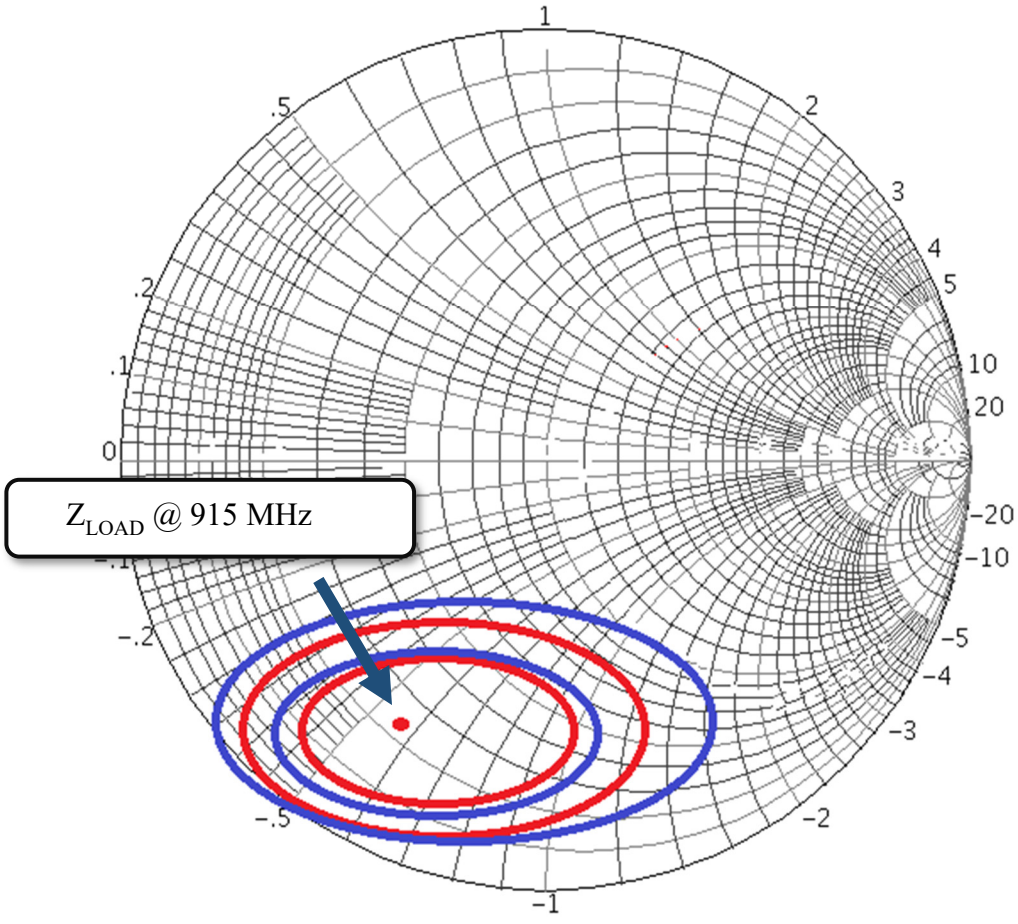


Figure 3.20: The load-pull analysis's power contours at 915 MHz [160]

3.9 Conclusion

The design and analysis of two novel PA architectures have been taken into consideration in this chapter. First is the proposed DPA design with fixed interstage capacitances. The frequency-dependent behaviour of passive parasitic components that affect the system performance is achieved. This architecture runs at a high frequency of 2.4 GHz. It explains a systematic approach to DPA design, including the specific architectural flow, building a schematic from an ideal, and utilizing actual components found in 65-nm CMOS technology to construct microstrip transmission lines. Before moving on to the next design step, which mostly included the layout, the key characteristics of the gadget that is available in the technological library are kept in mind. In addition to drain voltage supply and gate bias voltage, another important factor for a good ULP prototype is the impedance experienced by the device. With the help of an analysis including the change in gate bias voltage, the load-modulation and fixed inter-stage capacitances method are used to switch on the peaking amplifier at the proper moment. This increased the OBO of overall DPA design.

The second design represents an ET technique for RF PA with its power-utilisation mechanism. An ET supply bias with cascoded cells terminated as class-F in CG feedback have been proposed to maximize RF PA efficiency while consuming less DC power. In the simulations and experimental measurements, for a 2MHz BW signal at 915 MHz frequency band, the output BW is obtained at the best design. The linearity requirements of the system are discussed for rejection of OFDM harmonics and figure-of-merit is introduced to qualify the performance of RF PA. The cascaded linear technique, which uses an ED followed by a pre-amp, is superior than the traditional approach. If the input impedance is too low or there is a high bandwidth uplift and transconductance at the drain, the ED may load the pre-amp. The output impedance of the pre-amp is a few kilo-ohms or even less. As a result, the recommended ED design does not overburden the pre-amp. The load resistances (passive components) at the differential topology drain have also been removed to create additional chip area and save adequate amount of cost. The PA operate as two cascode cells terminated as class-F cells when gate-to-drain feedback is present. A common-source (CS) that serves as the transconductance stage and a common-gate (CG) with a fixed-bias gate-

voltage make up each transistor in a typical design. With a lowpass filter, the current combining method is used to combine the two cells.

The results for proposed ULP PA designs are analysed in next chapter.

CHAPTER 4

RESULTS AND ANALYSIS OF PROPOSED ULP PA DESIGN ARCHITECTURES

4.1 Overview

This chapter compares the pre and post layout simulation results for the proposed novel ULP PA design architectures. Sections 4.2 and 4.3 illustrates the results for ULP DPA with interstage capacitances and analyse the findings with state-of-the-art RF PA design architectures for short range & low power IEEE 802.15.4 WPAN standards. Section 4.4 to 4.8 illustrates the results for Class-F ULP PA using ET supply bias and analyse the findings with state-of-the-art RF PA design architectures for long range & low power IEEE 802.11ah WLAN standards. The pre and post layout results for output power, output gain, input insertion losses, DC power consumption and power-added efficiency are compared in tabular form with recent published results in top-tier journals.

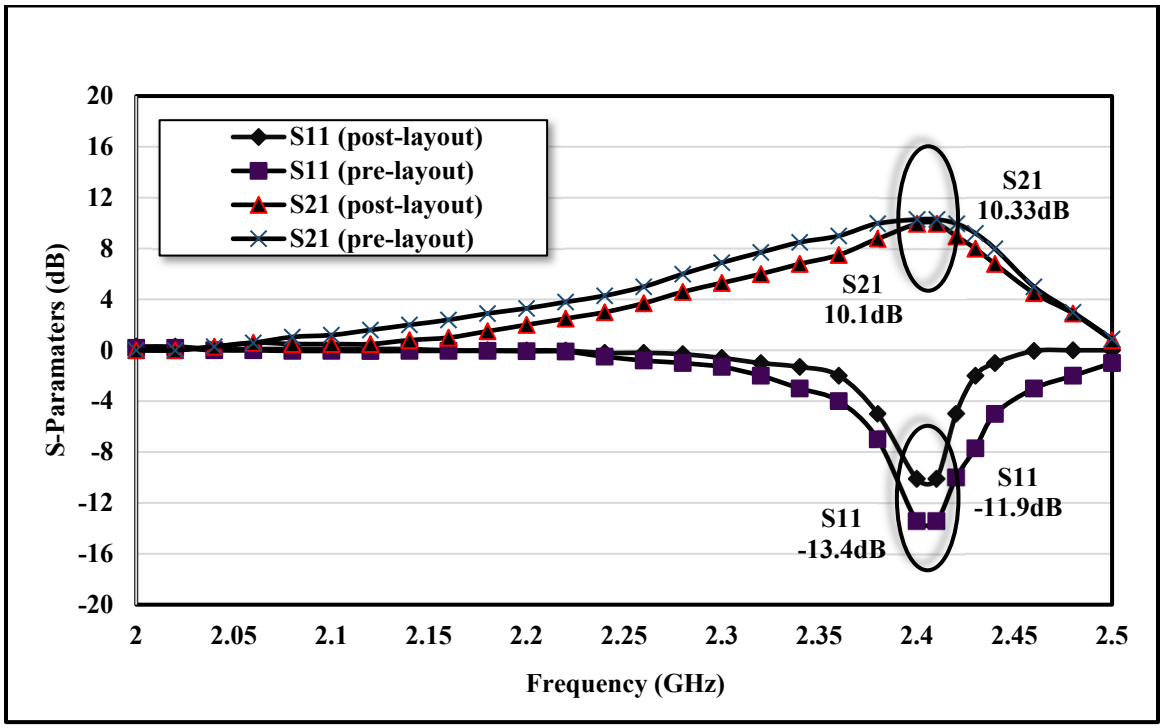
4.2 The Simulation Results for the Optimized ULP DPA Design

This section compares the pre- and post-layout findings. Figure 4.1(a) shows the input return loss (S11) and output gain. At centre frequency of 2.44 GHz, the PA exhibits a maximum gain of 10.3 dB and an input reflection loss (S11) of -13.4 dB. The 1-dB compression point, which is 4.1 dBm, is shown in Figure 4.1(b). The PAE is illustrated in Figure 4.1(c) which shows a post-layout efficiency of 29.2%.

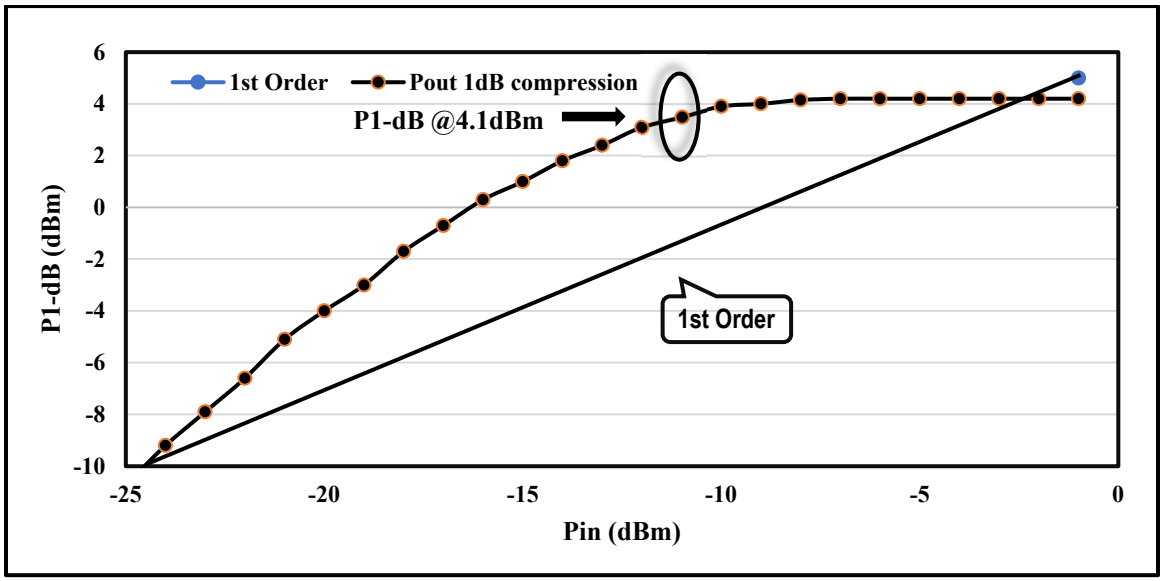
The Drain Efficiency (DE) is ratio of output power to the dc power delivered to the PA and is represented by η. The research focuses on DE to be plotted against OBO for three frequency ranges i.e., f_0, $0.75f_0$ & $1.25f_0$, and $0.5f_0$ & $1.5f_0$. Where f_0 is assigned 2.4GHz frequency band. The relationship between DE and OBO at various frequencies is depicted in Figure 4.1(d). According to the concept proposed in study ABC, efficiency is frequency independent during back-off, but only has a small frequency dependency during

maximum output power. Figure 4.1(e) compares the 1-stage and 2-stage PAE while observing the efficiency against the output power. The peaking amplifier contributes extra power at back-off, further increasing the overall DPA PAE. The plot shows an inflection point or "knee" at the OBO where auxiliary turns on and PAE rises to 29% peak value.

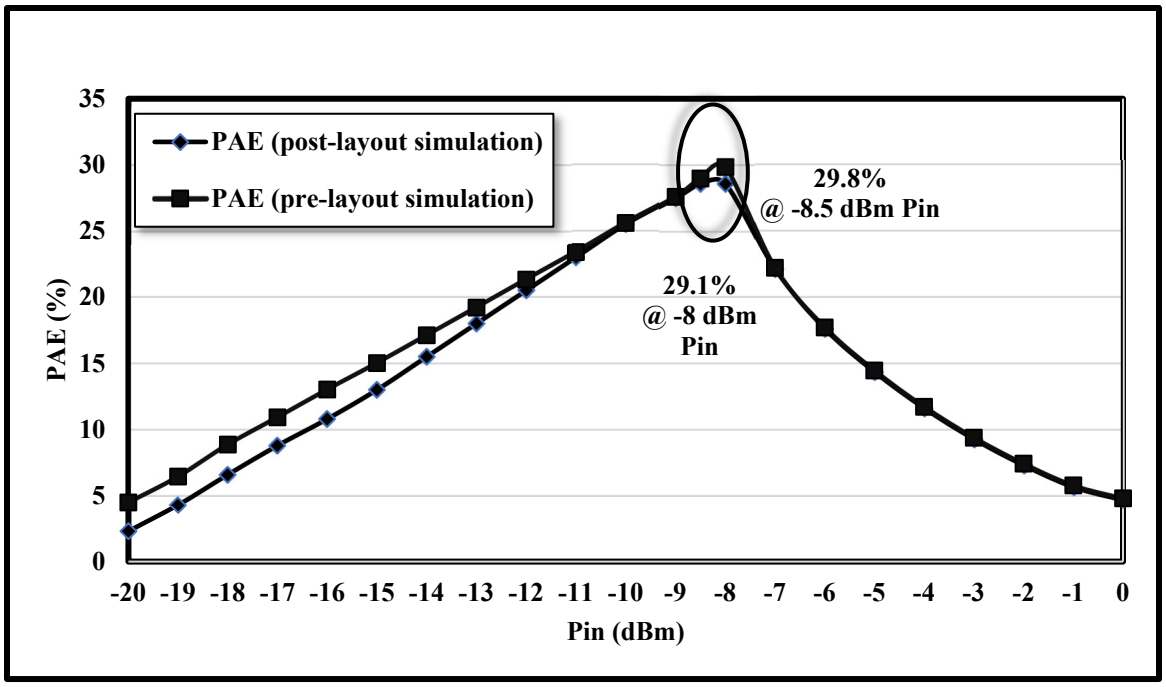
When both of the display windows results are combined along, the total power consumed by PA is 2.1mW. Two display windows are shown side by side in Figure 4.1(f). M1 biased in class-B has a 985.1µW DC power consumption (with drain current $I_{D(M1)}$ equals 547.5µA). M2 biased in class-C results in 1.194mW of DC power consumption (with drain current $I_{D(M2)}$ equals 663.5µA). This leads to overall DC power consumption for proposed ULP DPA to 2.1mW [146].



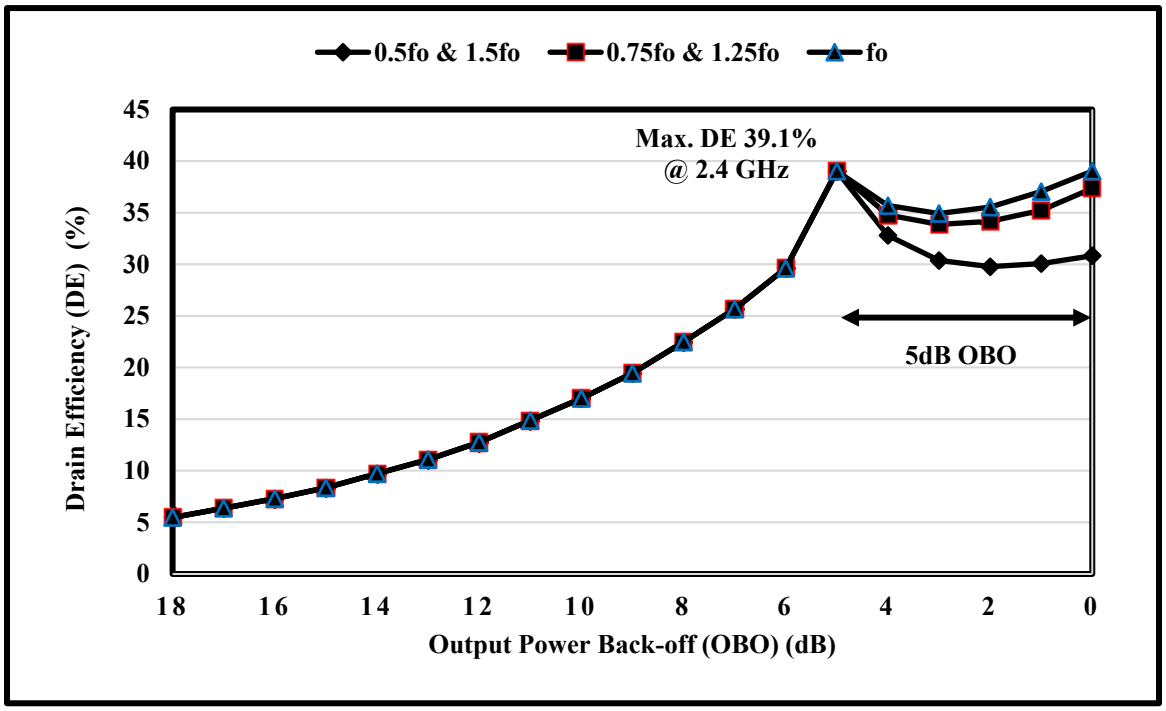
(a) Insertion-loss and gain



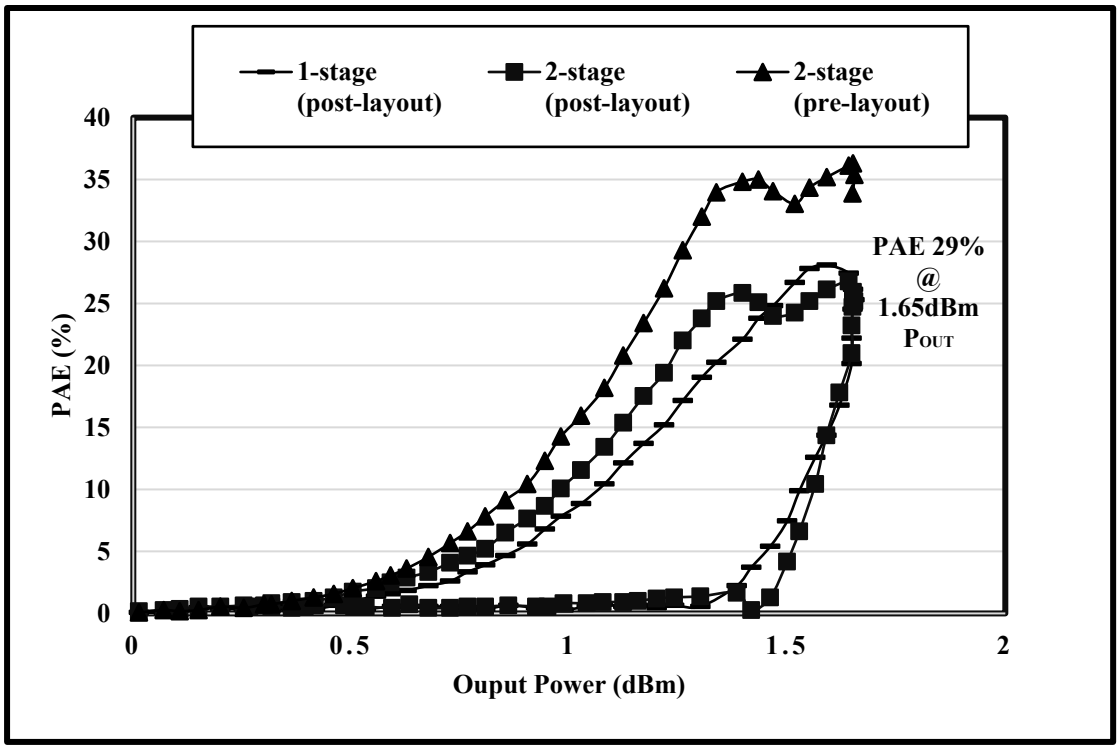
(b) P1-dB compression point



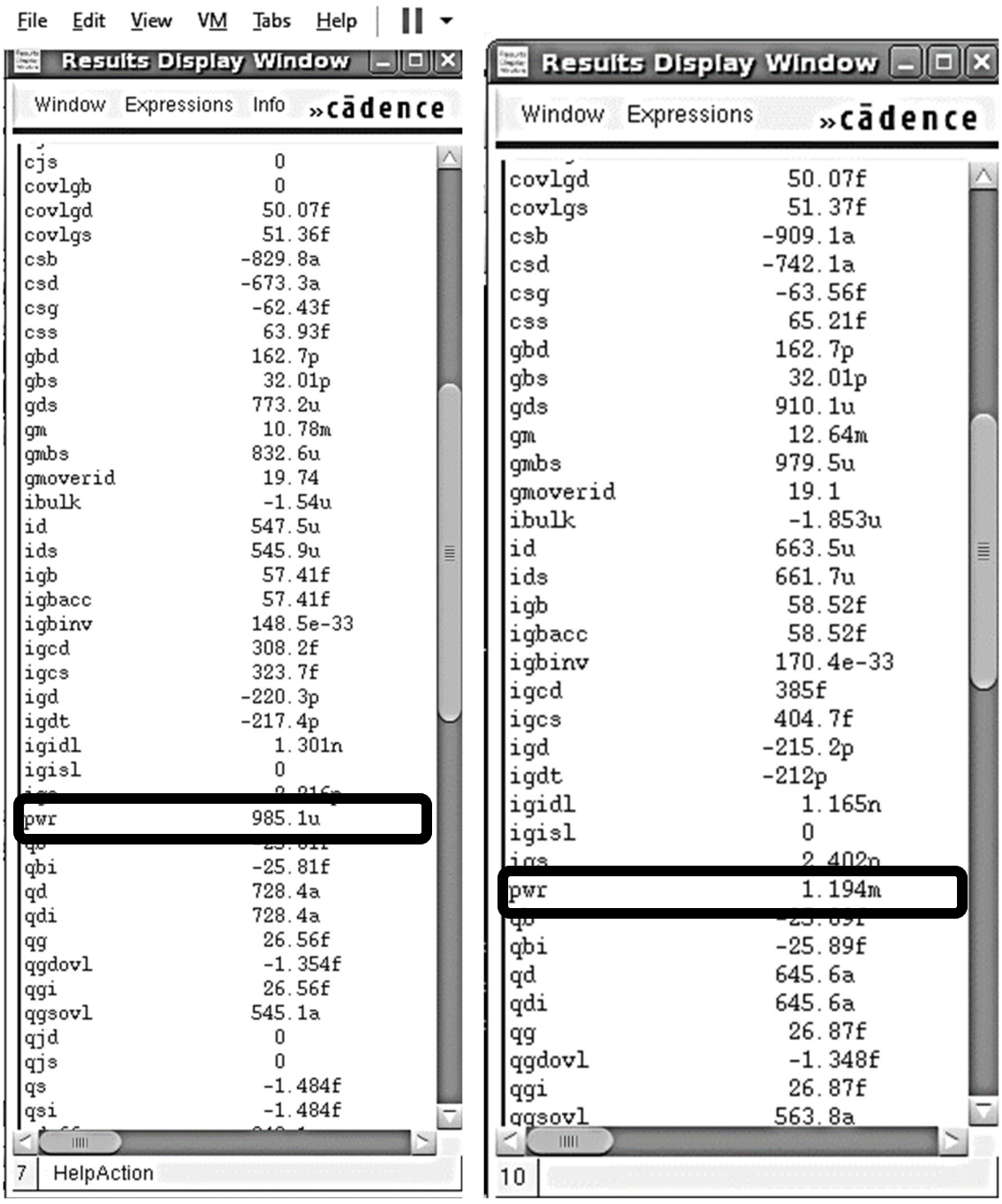
(c) PAE vs Input Power



(d) DE vs OBO plotted for frequencies from f_0, $0.75f_0$ & $1.25f_0$ and $0.5f_0$ & $1.5f_0$



(e) PAE comparison for 1-stage and 2-stage DPA with reference to the Output Power



(f) Overall DC power consumption

Figure 4.1: (a) Insertion-loss and gain (b) P1-dB compression point (c) Power Added Efficiency (PAE) vs Input Power (d) DE vs OBO plotted for frequencies from f_0, $0.75f_0$ & $1.25f_0$, and $0.5f_0$ & $1.5f_0$ (e) PAE comparison for 1-stage and 2-stage DPA (f) Overall DC power consumption of ULP DPA design as observed in simulation tool [146]

Although the response to the biasing approach looks not as ideal as expected in classical DPA simulation method. The magnitude of the fundamental current and voltage for the main device and the peaking device in response to rising input voltage is shown in Figure 4.2. We can see that the main voltage climbs linearly until it hits saturation in the low power zone below the transition or threshold point (~0.4V), while the main current likewise increases linearly, as predicted by theory, to reach a current of over 600µA. The high-power zone starts at the transition point voltage, and the fundamental current given by the peaking device increases from zero to practically the same maximum current as the primary device (or a little more than main device's current i.e., ~>600µA), while the voltage stays mostly linear. Keep in mind that some expansion is seen as a result of the main amplifier's compression as the input voltage rises and the device's less-than-ideal behaviour. The inputs provided to the CAD tool are generally preferred to be chosen as Pin. To get the perfection in statistical results for Figure 4.2, an equivalent values of input voltages have been deployed on horizontal axis by observing the peak and rms voltages from Figure 4.2. The similar input voltage ranges, from -20 dBm to -7 dBm which are in synchronization to PAE highest achieved values on pre- and post-layout simulations, are contrasted to input voltages for the statistical results of drain current and voltages, for the main device and the peaking device respectively.

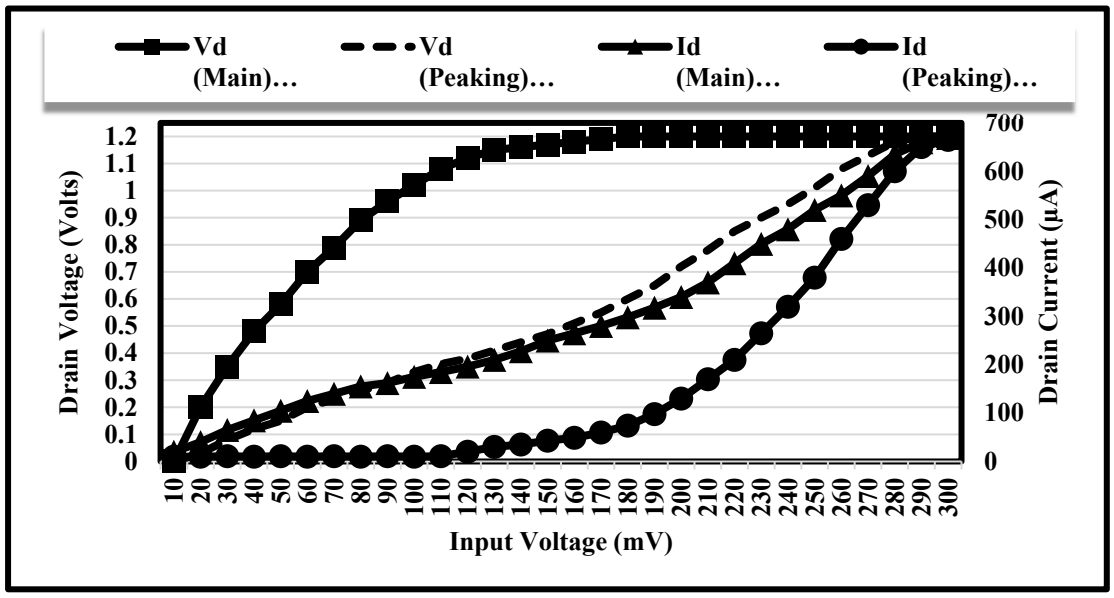


Figure 4.2: Response of the adaptive bias approach's drain current and drain voltage to the input voltage

4.3 Comparison of Performance Parameters of the Proposed ULP DPA with Current State-of-the-Art PAs for IEEE 802.15.4 WPAN Standard

Table 4.1 compares the designed ULP DPA performance PAs to state-of-the-art current CMOS PAs using 65-nm CMOS technology.

Table 4.1: Comparison of the proposed ULP DPA performance to state-of-the-art PA designs [146]

Specification	**This Work**		**[167]**	**[168]**	**[169]**	**[170]**	**[171]**
Technology	**65-nm**		65-nm	65-nm	65-nm	65-nm	65-nm
Year	**2021**		2021	2020	2018	2016	2016
IEEE Standard	**802.15.4 Zigbee**		802.11a WLAN/ 5G	802.15.1 Bluetooth	802.15.4 Zigbee	802.11n WLAN	802.15.1 Bluetooth
Frequency	**2.4 GHz**		5 GHz LP Mode/ 30GHz HP Mode	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz
Supply Voltages	**1.2 volts**		0.7 volts LP Mode	2.5 volts	1 volt	3.3 volts	3.3 volts
ULP/ LP	**ULP**		LP	LP	ULP	LP	N/A
DC Power Consumption	**Pre-layout**	**Post-layout**	---	---	1.9 mW	38 mW	171 mW
	2.14mW	**2.10mW**					
Output Power	**1.95 dBm**	**1.65 dBm**	1.1 dBm (LP)	25 dBm	-3 dBm	18.6 dBm	8.1 dBm
P1-dB Compression Point	**4.1 dBm**	**4.0 dBm**	3.1 dBm (LP)	---	---	---	12 dBm
Input Return Loss (S11)	**-13.4 dB**	**-11.9 dB**	-20 dB (LP)	---	---	---	---
Gain	**10.33 dB**	**10.14 dB**	11.5 dB (LP)	---	---	20.3 dB	13.5 dB
Peak PAE	**29.85%**	**29.2%**	16.5% (LP)	23.2%	26.2%	38.2%	16.5%
General Class of PA	**DPA with fixed inter-stage capacitances for 40MHz narrowband**		Multimode asymmetric PA	Doherty Class-G PA	PA-ADPLL	Class-B PA using 2:2 output transformer	Two stage (gain and programmable power) PA

PA has a non-linear tendency and the standards shown in published works provide simulation results using the standard frequency. This study has followed a similar pattern, as observed in Table 4.1. The aforementioned table concentrated on obtaining the findings using the standard 2.4GHz, while noting the centre-frequency in the range of 2.4GHz to 2.44GHz, with a bandwidth of 40MHz at most. The chart is arranged chronologically, beginning in the year 2021. The most recent top tier journals have been targeted for comparison of the post-layout simulated outcomes of this research. The IEEE 802.15 standards, which cover LP-WPAN devices, are used to compare these. The CMOS technology changes for different PA designs at the RF front-end from left to right. The DC power consumption in this study is less than that of the ULP designs that have previously been described. Another milestone in comparison to previously reported data is the output power level of 0 dBm. Excluding stage gains, the P1-dB compression point surpasses the 4dBm linear line, which is more than enough to generate a high-quality linear output consistent with other references. The value of 10.14dB in this case is more than enough to support this outcome as the minimum gain required to cross the optimum gain barrier is considered to be +10 dB. Since a FoM is a numerical metric that describes the performance of planned PA, it has been suggested to compare the post-layout simulated outcomes with earlier ones. It has a large chip, low DC power consumption, high gain, high output power, and minimal insertion or reflection losses.

4.4 Cost Projection Analysis for Proposed ULP DPA

The cost analysis of published papers in Table 4.1 on the design of CMOS Power Amplifiers (PAs) using 65-nm technology has been carried out in this section. The papers were analysed based on their published specifications including IEEE standards, frequency, supply voltage, ultra-low power/low power, DC power consumption, output power, input insertion loss, gain, peak power-added efficiency (PAE), general class of PA, number of transistors used, and area of design layout. Unfortunately, none of the papers disclosed the cost of their designed PAs. Therefore, based on the given specifications, a comparative analysis was carried out to predict which design could be most expensive and which could be least expensive. The cost of a PA is mainly determined by the number of

components used, the complexity of the design, and the manufacturing process. Therefore, based on these specifications, a comparative analysis was carried out to predict which design could be most expensive and which could be least expensive. The analytical reasoning for the cost projection has been provided in this section.

Study [168] has the highest area of design layout (1.6 square mm) among all the analysed papers. This implies that the design may require more components, leading to higher costs. Additionally, the design uses inductors to cover a large area, which may also increase the cost of the PA. Study [171] has the highest DC power consumption (171mW) among all the analysed papers. This implies that the design may require more power-hungry components, leading to higher costs. Furthermore, the design uses a two-stage gain and programmable power PA, which may also increase the cost of the PA.

On the other hand, this research has the lowest area of design layout (0.29 square mm) among all the analysed papers. This implies that the design may require fewer components, leading to lower costs. Additionally, the design uses only two transistors, which may also reduce the cost of the PA. Study [169] has the lowest DC power consumption (1.9mW) among all the analysed papers. This implies that the design may require fewer power-hungry components, leading to lower costs. Furthermore, the design uses an all-digital phase-locked loop (ADPLL) PA, which may also reduce the cost of the PA.

This study demonstrated a promising contribution to the field of RF PA, as it achieved an acceptable level of output power and PAE with only two transistors, low DC power consumption, and a small layout area. It is worth mentioning that this study's use of a Doherty PA with fixed inter-stage capacitances for 40MHz narrowband contributed to its cost-effectiveness. In conclusion, the cost of a CMOS PA design is heavily dependent on the design's complexity, the number of components used, and the manufacturing process. Therefore, researchers should strive to simplify the design, reduce the number of components used, and optimize the manufacturing process to reduce the overall cost of a CMOS PA.

4.5 The Simulation Results for the Optimized Class-F ET PA

The 65-nm CMOS technology has been used in design of the ET supply with class-F PA. Figure 4.3 illustrates the pre-layout and post-layout simulation results. The forward gain and insertion-loss are mentioned in Figure 4.3(a) i.e. -15.05 dB and +11.86 dB, respectively. The PA reaches a maximum efficiency of 37.1%, mentioned in Figure 4.3(b). The P-1dB compression point is expressed in Figure 4.3(c). The findings are compared via input frequency. An important metric for EDs is the conversion gain, which represents the efficiency of the down-conversion via the gain from RF to baseband frequencies in Figure 4.3(d). Equation (4.1) is used as a starting point to outline three primary affects that must be taken into account during design utilizing correction constants:

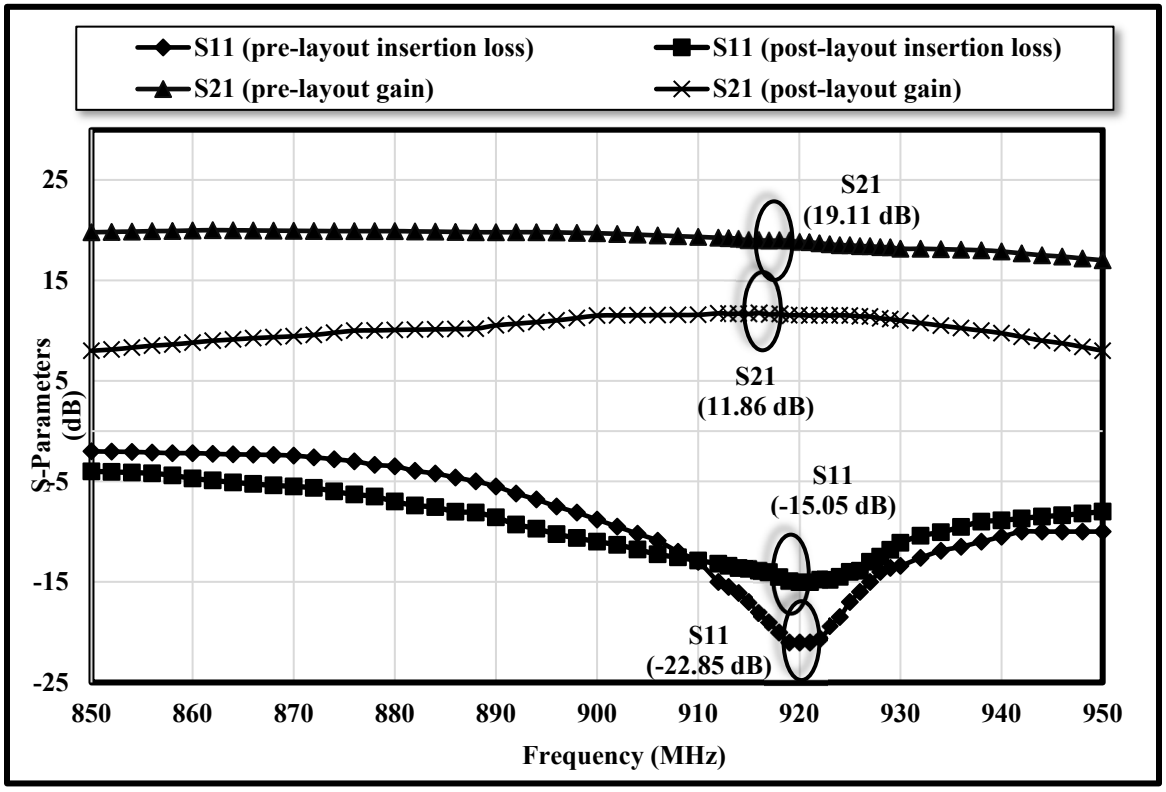
$$k = \frac{|V_{OD}|_{f=f_{Base}}}{V_{ID}|_{f=f_{Base}}} \tag{4.1}$$

where V_{ID} and V_{OD} are differential voltages at the input and output given by (4.2). The baseband frequency QAM modulated input signal is shown on f_{Base}.

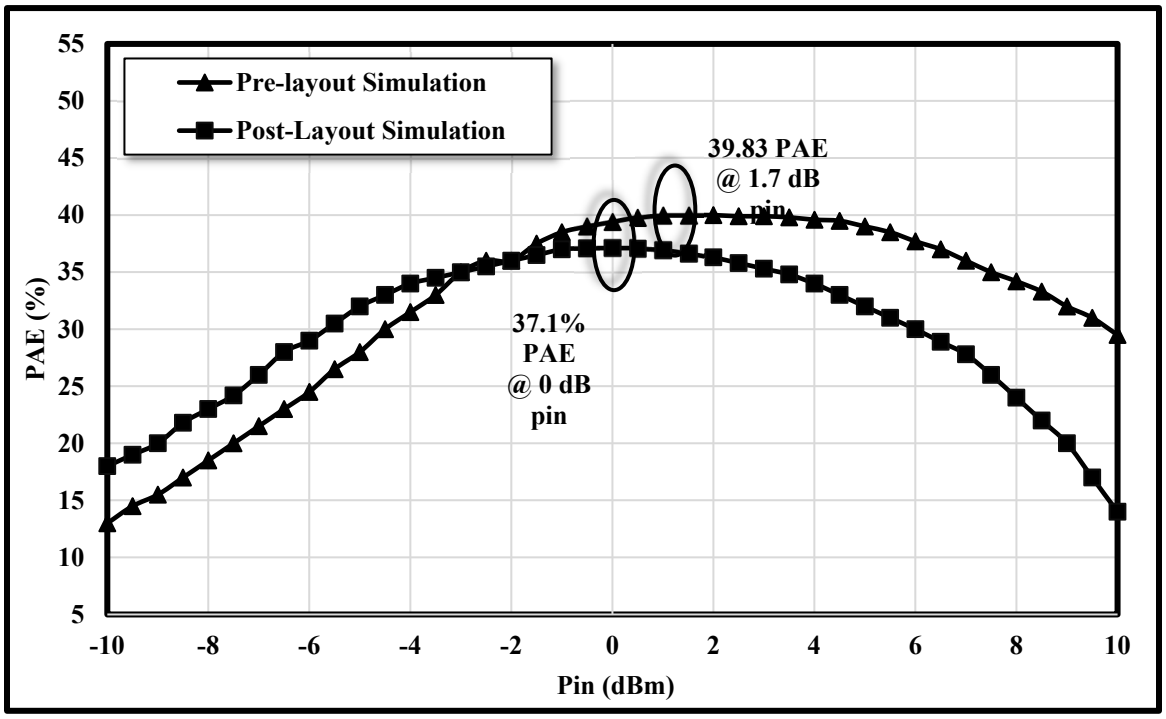
$$V_{OD} = V_0^+ - V_0^- = \frac{I_Q A^2 R_L}{4V_T^2} \tag{4.2}$$

Voltage (V_T) and amplitude (A) of the thermal signal are unaffected by the ED circuit design. As a consequence, the maximum conversion gain that may be obtained is limited by the quotient current (I_Q) and load resistance (R_L). The envelope detector is intended to provide a high conversion gain while having a broad input range. When the input power is 6 dBm, the suggested envelope detector achieves 57% of the maximum conversion gain. The peak voltage amplitude is taken into account for the equivalent input power provided to the envelope detector since the conversion is not expressed in decibels (dB), but rather as a normalized (or percent) value. Because the typical envelope detector solely consists of passive components, the conversion gain of the envelope detector is less than 1. Due to the impact of noise/power losses and offset values, the comparator is unable

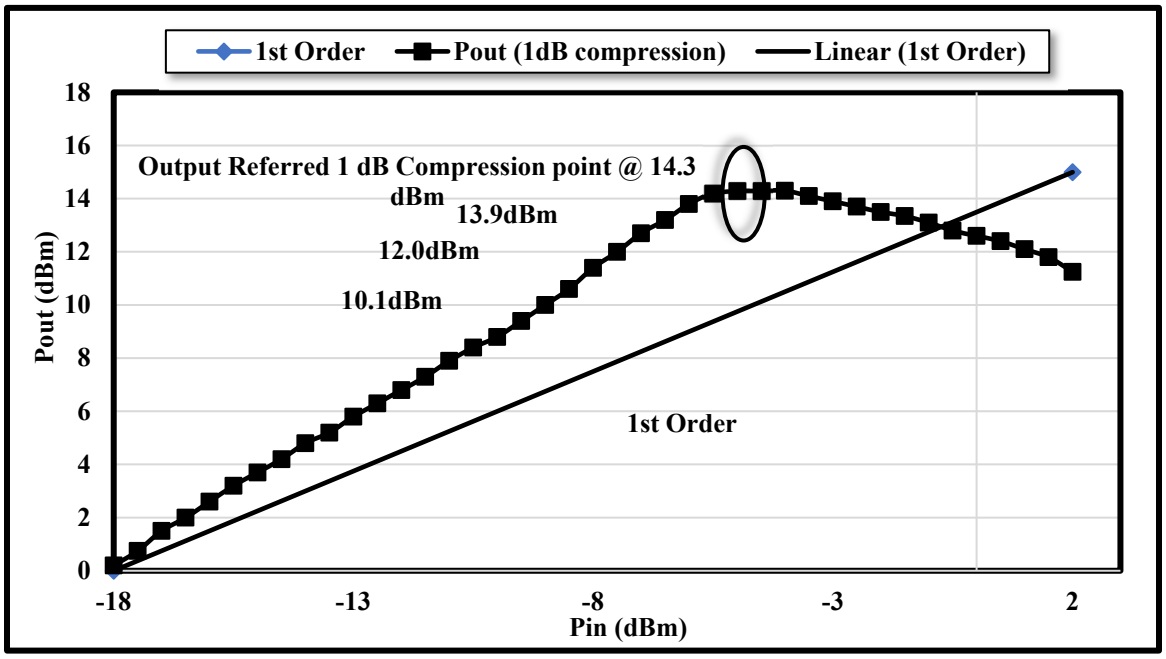
to provide accurate results when the modulation index of a QAM-based OFDM signal is low. Additionally, envelope detectors with active components like MOS transistors may provide significant conversion gain. For the OFDM baseband signal, the conversion gain has been examined in an open-loop setting. Strong inversion regions conduct substantially more current than weak or moderate inversion regions do for MOSFET. The majority of the current in our design comes from MOSFETs in the strong inversion zone. So, it becomes sense to approximate using the square law MOSFET model. Wide input range and high conversion gain cannot be simultaneously achieved under ULP consumption, according to the output current and transconductance characteristics [160].



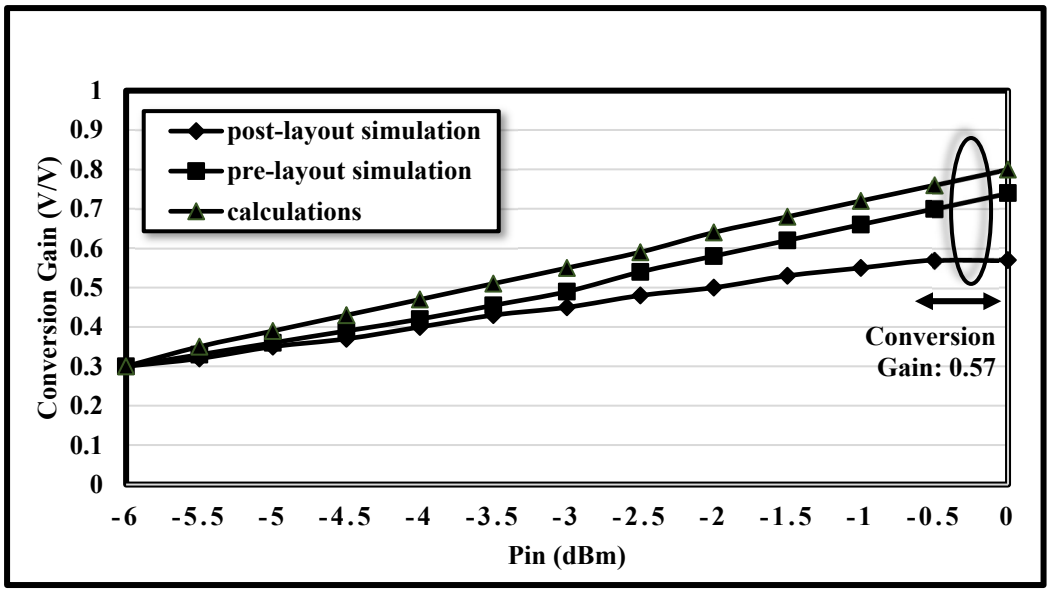
(a) Insertion-loss and gain



(b) PAE vs Input Power



(c) P1-dB compression point



(d) Conversion Gain (V/V)

Figure 4.3: (a) Insertion-loss and gain (b) Power Added Efficiency (PAE) vs Input Power (c) P1-dB compression point (d) Conversion gain (V/V) [160]

4.6 Power and Efficiency of ET PA using MATLAB as Behavioural Modelling

This section describes the graphical user interfaces (GUI) in the statistics toolbox that are used for evaluating probability distributions. Working with probability distributions is a key aspect of using statistics for data in simulation software includes three GUI's as well as command-line tools that make it easy to look at probability distributions, generate random samples from them or fit them to your data will discuss two of the GUI's briefly and then discuss the distribution fitting tool in more detail. The first GUI will introduce let us look at probability distributions and determine how their parameters affect their shape to open this GUI type of distribution tool at the simulation software command prompt. This GUI lets us select which of the twenty available distributions we want to look at and whether you'd like to view the probability density function or cumulative distribution function for the distributed data. We will look at the PDF for our normal distribution you can change the mean and standard deviation for the distribution and see how its shape changes. This GUI is excellent for developing an intuitive understanding of probability

distributions. The second GUI will introduce generates random samples from any of the twenty available probability distributions and displays the samples as histograms (or any other graph plot preferred). It also allows to export the random samples for the workspace which one can use to test hypotheses or models under different conditions to open this GUI type of "Random" tool at the simulation software's command prompt. First, we create 1 as the mean and 2 as the standard deviation characterizes a normal distribution, and generate random sample from it. The GUI creates and displays this sample in about a second. We click the resample button to generate another random sample and export the sample to the workspace. A cure-fitting tool at the command prompt, the distribution fitting tool lets you fit 16 predefined probability distributions or your own custom distribution to your data set. It makes it easy to pre-process your data set visually analyse fit quality compare multiple fits and evaluate fit results the distribution fitting tool has several task buttons for creating analysing and managing the distributions.

Getting the most out of the system is one of the key goals of the planned ET PA. When choosing an operating point and input/output parameters during the optimization process, an accurate power loss model is particularly helpful. Modern research publications use a variety of power loss models, including:

- Physics Modelling
- Behavioural Modelling
- Analytical Modelling

Physics-based models often contain a high degree of detail, which leads to computations that take a lengthy time in addition to being very accurate. The accuracy and calculation time of the behavioural model must be balanced, however without taking into account the static and dynamic nonlinear effects, accuracy issues may arise. The analytical model can provide simulations reasonably quickly and contain equations that account for the converter's non-ideal behaviour. A hybrid model that combines both the behavioural analytic loss model and the suggested PA's efficiency optimization is described in [172]. This paradigm offers several benefits, which may be summed up as follows:

- The model has decent ULP range accuracy (lower than 10mW).
- Due to their high frequency operation, n-MOS and p-MOS parasitic inductances are taken into consideration.

Analytical procedures include the nonlinear forward transconductance and nonlinear parasitic capacitances. The model's specifications for 65-nm CMOS technology may be found in the datasheets. It should be underlined that the model of nonlinear capacitors and changing transconductance is crucial for preventing significant estimate error in efficiency. With different equivalent circuits for each sub-period of transition, distinct state variables for each period, iterative numerical calculation of the state variables evolution with a fixed time-step, and consideration of the energy stored in parasitic component, it can be concluded that the main approach is this. The model separately analyses the high side turn-on and high side turn-off between high and low PAPR levels as the two primary transitional phases. Similar to previous tools, starting with the steady state circumstances at the start of the transitions, it is possible to determine the principal waveform and the losses. A purposefully clipped OFDM signal or an OFDM signal that operates in an amplifier's saturation region were both taken into account by [173]. Be aware that depending on the saturation level, these types of warped OFDM signals produce an error floor. The research looked at the PD of M-QAM-modulated OFDM signals. Theoretically, the continuous Gaussian PD of the mth OFDM symbol with N subcarriers is not present, and the PD is a function of m, where m ∈ [0,1..., N-1]. Additionally, it deduced the PD for illustrative situations of m ∈ [N/4, 2N/4, and 3N/4]. It presented a generic form of the PD for, m ∈ [0, N/4, 2N/4, 3N/4]. Figure 4.6 plots the simulation software tool results, where the linear power losses and the linear ET PA's efficiency are modelled. The efficiency of the ET PA is computed with the power loss of linear cascaded PA:

$$P_{converter} = \int P_{dist.}\left(v_{out}(t)\right).P(I_{out}, v_{out})dv_{out}(t) \tag{4.3}$$

$$P_{linear} = \frac{\int v_{out}(t)\big(v_{out}(t) - v_{in}(t)\big).dt}{R_L} \tag{4.4}$$

where $P_{dist.}$ is the probability distribution of envelope waveform $v_{out}(t)$, and $P_{converter}$ is the function observed as output voltage and current as seen from input to output stage. The simulation time for an envelope with a bandwidth of 16MHz is greatly reduced by this probability distribution-based technique for power-loss conversion. P_{linear} can be found using the original envelope and the full slow envelope if the overall resistance of load (main PA) is known.

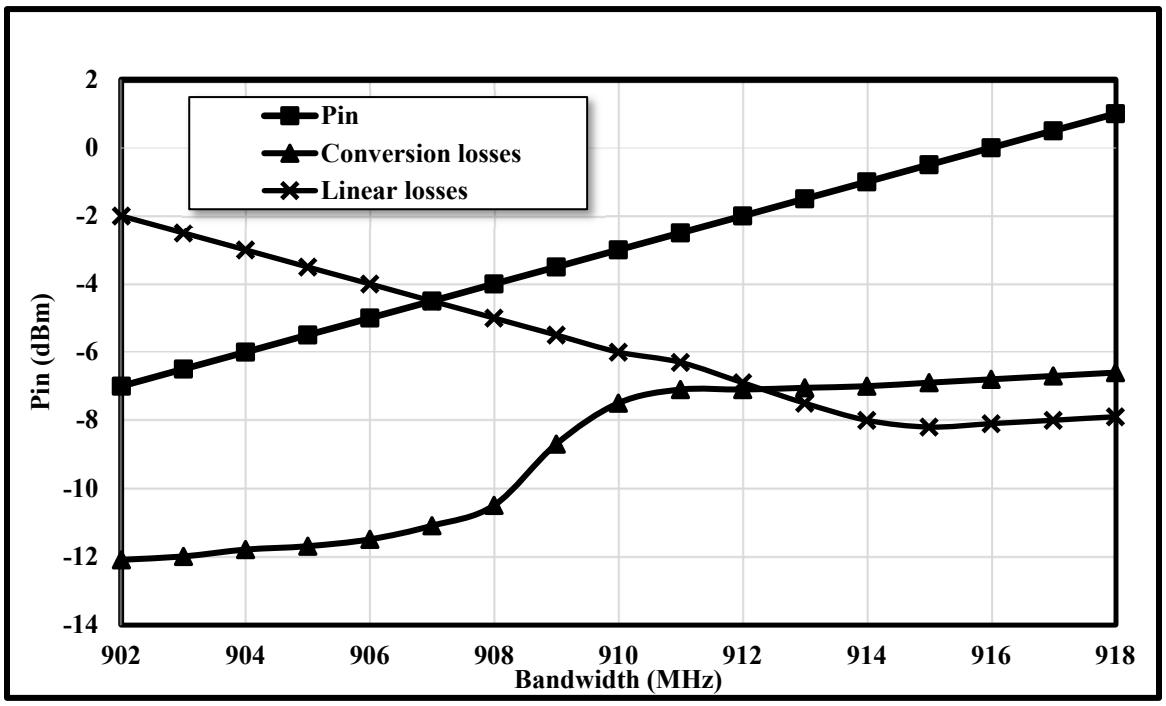


Figure 4.4: Power losses behaviour resulting from linear amplifier simulation software's stagnant (slower) envelope [174]

4.6.1 Current Efficiency vs the Current at the Output Load

Began with the establishment of the design equations and taking into account the limitations imposed by the application, the suggested regulator may be designed as follows:

- Obtain great current efficiency with small, medium, or large loads. Since the PA is in standby mode, which is known to as quotient current I_q, the total quiescent current of the regulator must be less than 1/100 times the supplied current, or around 0.3μA. Since the envelope consumes the most power of any block, the maximum bias current may be estimated. A minimum current efficiency of 60% was determined for the output current of 3.125mA in order to get the initial estimate of the total quiescent current of the envelope detector and its effects on the regulator performances. The PA is built with a nominal unregulated input voltage of 1.2 V and each transistor is intended to produce currents as shown in equations i_4 and i_5, which are maximum currents delivered at the drain outputs, taking into account the quiescent current of 0.3μA in the load resistor. We can show that the drain current grows exponentially with the huge input voltage by using the maximum values of $i_{4(max)}$ and $i_{5(max)}$. To maintain the transistor in the weak inversion region, which is necessary for ULP, the aspect ratio of M3 and the biasing voltage are, however, set. It is important to remember that none of the other transistors should be enlarged since doing so might result in higher drain current, which would place the transistors in a strong inversion area and throw the whole system out of balance.
- Once every bias condition has been determined, the compensation components may be calculated.

Figure 4.7 depicts how the current at the ED rises as the current at the PA load rises. The current efficiency is maintained at approximately 40% when the load current is more than 3mA, while the system assures a value of around 20% for low load current.

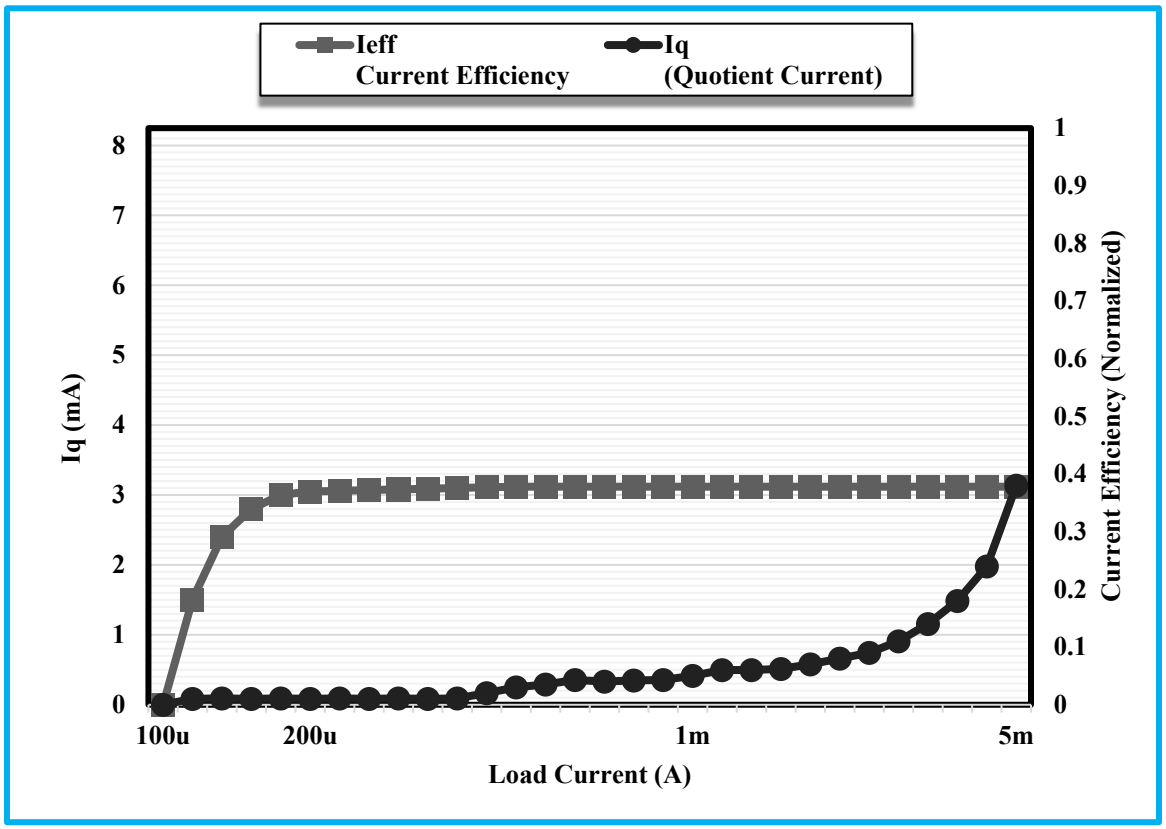


Figure 4.5: The current efficiency and quotient current on the load current scale. Only the operating mode is displayed in the trend. The lowest drain current required to keep the MOS device ON reduces the current efficiency in stand-by mode.

4.7 Comparison of Performance Parameters of the Proposed ULP ET PA with Current State-of-the-Art PAs for IEEE 802.11ah Standard

Table 4.2 compares the designed ULP ET PA performance to state-of-the-art current CMOS PAs using 65-nm CMOS technology.

Table 4.2: Comparison of the proposed ULP ET PA performance to state-of-the-art PA designs using 65-nm CMOS Technology

Specification	**This Work**	**[175]**	**[176]**	**[167]**	**[168]**	**[177]**	**[178]**	**[169]**	**[170]**	**[171]**
Technology	**65-nm**	65-nm	65-nm	65-nm	65-nm	180-nm	180-nm	65-nm	65-nm	65-nm
Year	**2022**	2022	2021	2021	2020	2020	2019	2018	2016	2016
IEEE Standard	**802.11ah**	802.11ah	802.11g WLAN	802.11a WLAN/ 5G	802.15.1 Bluetooth	802.11ah	802.11ah	802.15.4 Zigbee	802.11n WLAN	802.15.1 Bluetooth
Frequency	**Sub-1 GHz (915 MHz)**	Sub-1 GHz (960 MHz)	2.4 GHz	5 GHz LP Mode/ 30GHz HP Mode	2.4 GHz	Sub-1 GHz (986 MHz)	Sub-1 GHz with two modes of operation LFM: 0.4-0.6 GHz HFM: >0.6 GHz	2.4 GHz	2.4 GHz	2.4 GHz
Supply Voltages	**1.2 volts**	2.4 volts	1.2 volts	0.7 volts LP Mode	2.5 volts	1.8 volts	1.8 volts	1 volt	3.3 volts	3.3 volts
ULP/ LP	**ULP**	ULP	ULP	LP	LP	ULP	ULP	ULP	LP	None of these
DC Power Consumption	**3.75mW**	---	3mW half-duplex (HD) and 6mW full-duplex (FD) operations	---	---	---	4.7 mW	1.9 mW	38mW	171mW

Output Power	**14 dBm with Saturated Output Power of 22 dBm**	17 dBm	21 dBm	1.1 dBm (LP)	25 dBm	14.2 dBm with saturated output power of 24.2 dBm	12.73 dBm with Saturated power of 20.15 dBm	-3 dBm	18.6 dBm	8.1 dBm
P1-dB Compression Point	**14.3 dBm**	---	---	3.1 dBm (LP)	---	---	---	---	---	12 dBm
Input Return Loss (S11)	**-15.05 dB**	---	-16 dB	-20 dB (LP)	---	---	---	---	---	---
Gain	**11.86 dB**	---	----	11.5 dB (LP)	---	---	---	---	20.3 dB	13.5 dB
Peak PAE	**37.1%**	42.7%	26.5%(HD) 17.4%(FD)	16.5% (LP)	23.2%	48.1%	25.6%	26.2%	38.2%	16.5%
General Class of PA	**Class-F with feedback using ET supply-bias**	Class-D Switched Capacitor PA	Quadrature Band-Switched Capacitor PA	Multimode asymmetric PA	Doherty Class-G PA	Class-D	Reconfigurable/ Switchable balun/TF with drain-bias configuration	PA-ADPLL	Class-B PA using 2:2 output transformer	Two stage (gain and program-mable power) PA

The behaviour of PA is non-linear. The standards observed in published articles shows the simulation results using the standard frequency and the similar trend has been followed in this research. Believing in mentioning the centre-frequency in the band of 915 MHz to 931 MHz, with bandwidth of 16MHz at maximum, this thesis focused on deriving the results using the standard 915 MHz for US standards only. The table is set in chronological order, starting from year 2022 and not before year 2018. Results older than five years have not been contrasted and only state-of-the-art top tier journals have been targeted to compare simulated results. These are compared upon IEEE standards for long-range and low-power WLAN devices under the umbrella of 802.11ax standards. The CMOS technology varies from left to right for various PA designs in RF front-end. The DC power consumption in this research is lower than the previously reported ULP architectures. The output power when comes to saturation, reaches to 20 dBm, which is another a milestone in contrast to previous published results. The P1-dB compression point, excluding the gain of stages, exceeds the 14 dBm linear line, which is quite sufficient to produce a quality linear output in-line to other references. The minimum gain to surpass the ideal gain barrier is assumed to be +10 dB, and here the value of 11.86 dB is quite sufficient to justify this result. A FoM has be proposed to contrast the post-layout simulated results with previous ones as it is a numerical measure which characterizes the performance of designed PA. It includes a high gain, high output power, but a very low DC power consumption, size of chip and insertion or reflection losses [174].

4.8 Cost Projection Analysis for Proposed ULP ET-PA

This section presents a cost projection analysis of published research articles in Table 4.2 on CMOS Power Amplifier designs using 65-nm technology. The cost of the design is a crucial factor that determines the feasibility of the amplifier in practical application. Unfortunately, research articles do not disclose the exact cost of their designed power amplifiers. Therefore, this section aims to provide an estimation of the cost of these designs based on their technical specifications. The analysis is based on the power consumption, output power, peak power-added efficiency, general class of the amplifier,

number of transistors used, and the area of design layout. The results show that [171], which has the highest DC power consumption of 171mW, and [168], which uses inductors that cover a large area, could be expensive to manufacture. On the other hand, this work for ULP ET-PA, which has the lowest DC power consumption of 3.75mW, and [169], which has a small area of design layout, have probabilities of less expensive to produce.

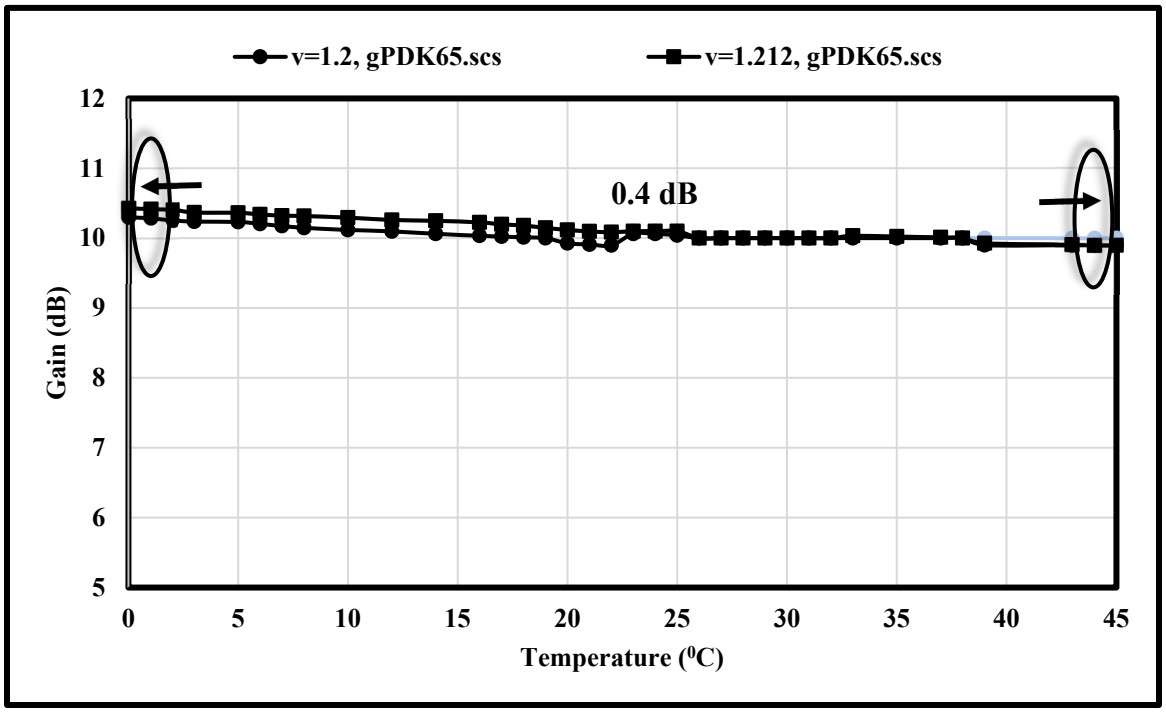
The PA class indicates the design topology used to amplify the signal. A higher PAE implies a more efficient amplifier design, which reduces power consumption and thermal management requirements. The number of transistors and the area of design layout indicate the complexity and size of the design.

The research findings suggest that the CMOS PA design presented in this work for ET-PA design, could potentially provide a cost-effective solution in the field of RF PA. Moreover, the cost of a CMOS PA using 65-nm technology appears to be largely dependent on factors such as the number of components involved, design complexity, and the overall manufacturing process. These factors must be taken into account when estimating the cost of manufacturing such PA designs. The conclusion drawn from this study aligns with the consensus in the field that the cost of a PA design is a critical factor that needs to be considered during the design process, especially when targeting low-cost applications.

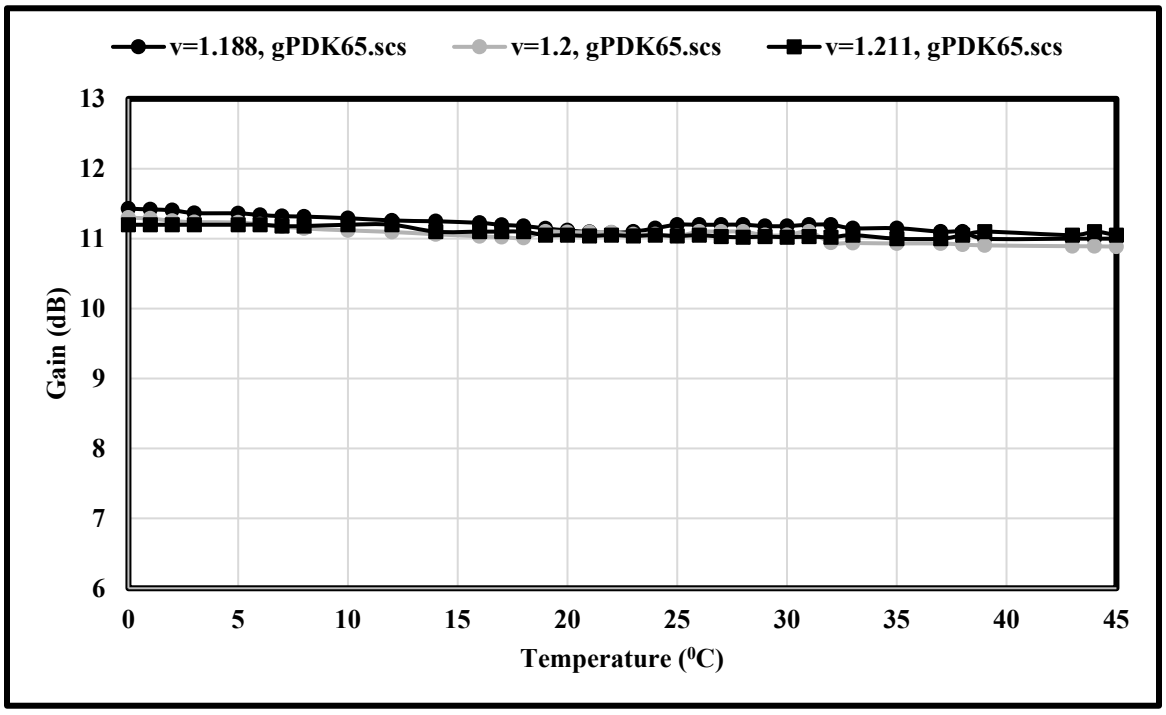
4.9 Process-Voltage-Temperature (PVT) Variations for Simulation Results

This subsection illustrates the process-voltage-temperature (PVT) analysis and variations for parameters of proposed ULP PA designs. The choice of PVT corners for a CMOS RF PA design depends on several factors, including the technology node, the specific design requirements, and the expected operating conditions. Study [179] shows some general guidelines for choosing PVT corners for CMOS technology. The process is marked slow (SS) for the design which requires low power consumption, voltage to typical as the design needs to operate under low-power supply conditions and the temperature to typical as the design is intend to use in temperature controlled or room temperature environment. The analogue design environment launches the global voltage variable V_{DD} with 1.2 volts which is further varied. The corner setup adds corners from two typical corners which are used to verify the performance of PA designs. The two convention letters

of corners (C0 and C1) represent are performance of n-MOS. Since there is no p-MOS used, so selecting the fast (FF) variable show no means. The aforementioned process controls are selected on process-development-kit (PDK) model file for analysis. The process chosen SS (slow) at C0 defines the process is less than the typical threshold or subthreshold regions. Additionally, the process of NN (nominal) at C1 is considered as an alternative process-variation test. NN shows the nominal or ideal bench test. The voltage variations are assumed with 10 percent tolerance showing the ranges: 1.188 to 1.212 volts. These ranges are similar to all two corners and ae set as 1.188, 1.2, 1.212. Temperature ranges are assumed to be from 0 to 45 degrees (0, 25,45). The voltages and temperature values are placed in both corners C0 and C1. Figure 4.8(a) and 4.8(b) shows the gain variation of DPA and ET PA with the change in temperature on aforementioned range respectively. As observed the change in gain is only 0.4 dB for DPA and 0.9 dB for ET PA [174].



(a) The gain variation of DPA with temperature



(b) The gain variation of ET PA with temperature

Figure 4.6: The gain variation of DPA and ET PA with the change in temperature during PVT analysis [180]

4.10 Conclusion

This chapter shows the simulation results for the proposed CMOS RF PA design architectures. Section 4.2 and 4.3 analyses the simulation results for ULP DPA using interstage capacitances. The novel design shows 2.1mW ultra-low DC power consumption, 29.2% PAE, and 4 dBm P1-dB compression point. The post-layout simulations show an extremely high gain of 10.14 dB, very low input-insertion loss of -11.9 dB, very strong drive current capability of 547µA & 663µA for main & peaking PAs respectively. Impedance matching is acquired to achieve the desired harmonic suppression at the output of DPA design. The post-layout simulations show consequences in comparison to state-of-the-art PA architectures for ZigBee and similar devices under low-power wireless personal area network (WPAN).

Sections 4.4 to 4.8 analyses the simulation results for ULP ET supply with class-F PA. The novel design meets the requirements of the IEEE 802.11ah standard for long-range low power WLAN by using a DC power consumption of 3.75mW, a PAE of 37.1%, and an operating frequency in the unlicensed 915-931 MHz band in the United States. The chip layout size is reduced to just 0.13mm^2 by the inductor-less design for ET supply bias.

As compare to DPA results, ET PA shows very good results in terms of the output power and the efficiency. One of the reasons is the IEEE standard which limit the output power not less than the findings due to its specifications. A mathematical model showing the behaviour of power loss has also been discussed in this chapter, where the probability distribution of envelope waveform voltages & converter power functions is observed as output voltage and current as seen from input to output stage. The results have been compared with recent articles published in top tier journals. It includes power gain, output power, input insertions losses and PAE as major parameters. Although no mathematical relationship for FoM has been suggested for comparison of results, however, the correlation between the values, especially the DC power consumption shows some contribution to this research.

CHAPTER 5

DISCUSSION AND CONCLUSION

5.1 Implications of the Study

The DPA approach was chosen in this study as a promising alternative for 2.4 GHz wireless communication IEEE 802.15 standards to achieve adequate linearity under ULP consumption. Although DPAs have traditionally been employed in narrowband contexts, efforts have recently been made to increase their bandwidth in an effort to overcome the difficulties associated with high efficiency RF radio systems. Conversely, to increase the PA average efficiency for high PAPR signal, the ET is a potential efficiency improvement strategy. A WLAN application under 802.11ah IEEE standard requires high linearity PAs due to the high PAPR statistic features. Traditionally, Class-A or Class-AB PAs are backed-off to create linear PAs. The intrinsic trade-off between efficiency and linearity for PA designs is shown by the fact that the average efficiency for a high PAR signal is substantially lower than the peak efficiency. The ET supply bias technique with cascode cells terminated as class-F in GD feedback is implemented to increase PA efficiency and rejection of OFDM harmonics under ULP operation.

5.2 Summary of Contribution and Practical Implications of Study

The doctoral dissertation successfully addresses the goals set forth in this thesis by developing novel designs for ultra-low power (ULP) RF CMOS power amplifiers. The research encompasses the design and optimization of a ULP Doherty Power Amplifier (DPA) for short-range and low-power IEEE 802.15.4 WPAN standard, as well as the design and optimization of an Envelope Tracking (ET) Supply Bias with Cascoded Cells

terminated as Class-F ULP-PA for long-range and low-power IEEE 802.11ah WLAN standard.

The initial objective of the research was to develop a traditional DPA architecture using ideal input sources and discrete components from analogue library. The proposed design, specifically targeted for the 2.4 GHz ISM band with a bandwidth of 40 MHz, served as a fundamental exploration of DPA design principles. While the obtained results lacked optimization, they provided insights into the design challenges and laid the foundation for further analysis and improvement.

To achieve a prototype with real components, the design was optimized using the components available in the CAD tool library. One key aspect of this design was the implementation of tuned fixed interstage capacitances to enhance the ULP DPA's narrowband performance, while being biased in the subthreshold region. The measurement procedure was executed in a real-world design environment, incorporating two independent input sources connected to the main and peaking amplifiers, enabling the evaluation of DPA performance. The dissertation's focus on load modulation and its impact on Doherty efficiency and performance at extremely low power is a significant contribution. Techniques for perfect matching using small signal analysis and diagram charts were employed to enhance linearity and efficiency under low-power operations. The study presents a systematic approach to DPA design, emphasizing architectural flow, schematic development from ideal sources, and the utilization of actual components in the 65-nm CMOS technology library for microstrip transmission line construction.

The dissertation also explores a novel ET supply bias technique with cascode cells terminated as Class-F in GD feedback, specifically targeting sub-1 GHz, IEEE 802.11ah low-power and long-range OFDM-based WLAN applications. By investigating the challenges faced by narrowband ET PAs, including Fourier analysis of OFDM harmonics through the RF input, a proposed topology was implemented and optimized using Class-F with gate-to-drain feedback. The ET supply bias successfully incorporated a cascaded linear pre-amp with envelope detection, presenting an inductor-less design that significantly reduced chip area compared to the DPA design.

Both the DPA and ET architectures were realized using real components in the CAD tool based on 65-nm CMOS technology. The pre-layout and post-layout simulations

were performed, resulting in notable improvements in power-added efficiency, particularly for WLAN OFDM signals. Comparative analyses with state-of-the-art ULP-PA designs published in top-tier journals showcase the merits of the proposed designs, with the ET PA demonstrating superior output power and efficiency.

The conclusion also highlights a mathematical model that examines power loss behaviour, observing the probability distribution of envelope waveform voltages and converter power functions. Although no specific mathematical relationship for Figure of Merit (FoM) is proposed for result comparison, the correlation between values, particularly DC power consumption, contributes to the advancement of this research.

5.3 Limitations of the Research

There are several limitations to conduct research on ULP RF CMOS power amplifiers. One major limitation is the lack of research infrastructure, which includes research labs and fabrication facilities, which are necessary for the production of IC chips. The tape-out results are not validated due to this limitation.

Another limitation is the lack of funding and resources for research. Developing countries like Pakistan may not have the same level of investment in research and development as more developed countries, which limits the ability of this study to conduct high-quality research and access state-of-the-art tools and equipment.

Overall, the lack of research infrastructure, expertise, funding, and resources can pose significant challenges to conduct research on ULP CMOS RF power amplifiers in developing countries like Pakistan. However, there is a minor possibility for collaboration with research groups in western countries, including European or the United States.

This research on ULP RF CMOS power amplifiers faces several limitations that need to be acknowledged. A significant constraint is the lack of research infrastructure, including research labs and fabrication facilities necessary for IC chip production. Due to this limitation, the tape-out results could not be validated.

Another limitation stems from the lack of funding and resources for research, particularly in developing countries like Pakistan. The limited investment in research and development restricts the ability to conduct high-quality research and access state-of-the-

art tools and equipment. However, there is a possibility for collaboration with research groups in more developed countries, such as those in Europe or the United States, which could partially mitigate this limitation.

Overall, the scarcity of research infrastructure, expertise, funding, and resources poses considerable challenges for conducting research on ULP CMOS RF power amplifiers in developing countries. Recognizing these limitations, further efforts should be directed towards seeking collaborations and accessing international research networks to enhance the quality and scope of future studies.

5.4 Future Perspective

The landscape of ULP RF IC designs is poised for transformative advancements, driven by emerging technologies, evolving standards, and the pursuit of energy-efficient wireless communication. As we look ahead, several key areas demand attention to shape the future trajectory of ULP RF IC designs.

5.4.1 Energy Harvesting Integration

The integration of energy harvesting techniques within ULP RF IC designs stands out as a promising avenue for future exploration. Leveraging ambient energy sources, such as solar, kinetic, or RF energy, presents an opportunity to enhance the autonomy of battery-powered devices. Collaborative efforts between RF IC designers and energy harvesting specialists could yield innovative solutions that extend the operational lifetime of wireless devices, particularly in remote or resource-constrained environments.

5.4.2 Machine Learning and Cognitive Radio

The synergy between ULP RF IC designs and machine learning algorithms holds immense potential for optimizing wireless communication systems. Cognitive radio, empowered by machine learning capabilities, can dynamically adapt to changing RF environments, optimizing energy consumption and spectral efficiency. Future research should delve into the seamless integration of machine learning algorithms within ULP RF ICs to enable adaptive and intelligent wireless communication systems.

5.4.3 5G and Beyond

As the telecommunications landscape evolves with the rollout of 5G networks, ULP RF IC designs will play a crucial role in meeting the stringent power consumption requirements of IoT devices within these networks. Looking beyond 5G, the development of ULP RF ICs must anticipate the demands of future wireless communication standards. Research endeavours should focus on enabling energy-efficient communication protocols, advanced modulation schemes, and smart sleep-wake strategies to align with the trajectory of evolving wireless standards.

5.4.4 Security and Trustworthiness

With the proliferation of IoT devices, ensuring the security and trustworthiness of ULP RF ICs becomes paramount. Future designs should incorporate robust security mechanisms to safeguard sensitive data and prevent unauthorized access. Exploration of hardware-based security solutions, resilient against emerging threats, will be integral to the long-term success and adoption of ULP RF ICs in diverse applications.

5.4.5 Cross-disciplinary Collaboration

The future of ULP RF IC designs necessitates cross-disciplinary collaboration. Bridging the gap between RF engineering, material science, and nanotechnology can open new frontiers. Collaborative research initiatives should seek to explore novel materials, fabrication techniques, and design paradigms to push the boundaries of ULP RF IC capabilities.

The future perspective of ULP RF IC designs is marked by a convergence of technological advancements and interdisciplinary collaboration. Researchers and industry practitioners should collectively strive to address the challenges posed by energy constraints, security concerns, and the dynamic nature of wireless communication environments. By embracing emerging technologies and fostering collaborative endeavours, the field of ULP RF IC designs is poised to make substantial contributions to the efficiency and sustainability of next-generation wireless communication systems.

5.5 Sustainable Development Goals (SDGs) Mapped with this Research

The proposed designs of ULP CMOS RF PA are mapped to several Sustainable Development Goals (SDGs), including:

SDG 7: Affordable and Clean Energy – The proposed ULP CMOS RF PA design will help reduce energy consumption and will contribute to the development of more energy-efficient wireless communication systems.

SDG 9: Industry, Innovation, and Infrastructure - The design of proposed ULP CMOS RF PA requires innovation and advanced manufacturing processes. This can support the development of sustainable infrastructure and industries, particularly in the areas of wireless communication and IoT devices.

SDG 12: Responsible Consumption and Production – The study can help reduce the environmental impact of wireless communication systems by minimizing power consumption, which in turn reduces the demand for non-renewable energy sources.

SDG 13: Climate Action - By reducing power consumption, it can help mitigate the impact of climate change and contribute to efforts to reduce greenhouse gas emissions.

SDG 17: Partnerships for the Goals - The proposed RF PA designs require collaboration and partnership between different stakeholders, including researchers, manufacturers, and policymakers. These partnerships can help ensure that sustainable design practices are implemented in the development of wireless communication systems.

In summary, the novel designs of ULP CMOS RF PA contributes to several SDGs, including affordable and clean energy, industry innovation and infrastructure, responsible consumption and production, climate action, and partnerships for the goals. These contributions are made possible through the use of sustainable design practices that prioritize energy efficiency and reduce the environmental impact of wireless communication systems.

5.6 Artificial Intelligence (AI) and CMOS RF PA Design

The future of RF CMOS power amplifiers (PAs) is likely to include increased use of artificial intelligence (AI) techniques in the design process. AI can help optimize and automate various aspects of the design process, such as circuit layout, parameter selection,

and model training. One potential application of AI in CMOS RF PA design is the use of machine learning algorithms to predict PA performance and optimize PA design for specific applications. For example, AI could be used to predict the PA's power output, efficiency, and linearity based on input parameters such as the operating frequency, load impedance, and bias conditions. Additionally, AI can be used to improve the reliability and robustness of RF PAs. Machine learning algorithms can be used to analyse and detect failures in the PA, and can even predict when a failure might occur based on various parameters such as temperature and bias conditions. This can lead to improved performance and reduced downtime in applications that require high reliability, such as aerospace or medical applications. Overall, the use of AI in CMOS RF PA design is a rapidly growing area of research and development, and is likely to play an increasingly important role in the future of RF PAs.

5.7 Conclusion

Even though a number of techniques for ULP design have been offered, contributions to achieve optimal solution are rare. Technology advancement has given more for less for a few decades. With each successive technological generation, less space and power per operation remained needed for a given performance. As a result, we now live in the smartphone, GPS, and Internet of Things age. Advanced scaling and ULP methods, on the other hand, put a stop to the fairy tale: increasing leakage and technical uncertainty make the more for less paradigm more challenging. We must deal with the energy performance trade-off in a much more active and purposeful manner now, and in the foreseeable future. Advanced design techniques, and precise ULP designs, optimum voltage supplied selection, and advanced architectural techniques to deal with timing variability, are all required to deal with timing variability. For it to stay relevant in the subthreshold areas, research into the influence of voltage supplied would be useful, particularly if generic rules could be found. Operating at a subthreshold voltage supplied allows for a review of previous findings. The growth of modern wireless communication networks toward datacentric services has resulted in the emergence of signals with high PAPR, exact linearity standards, and enormous modulation bandwidth. Carrier aggregated

signals will be used in future wireless standards to substantially increase transmission capacity. Therefore, RF PAs are required to efficiently and linearly amplify multi-band modulated signals with high PAPR dispersed across a broad frequency range.

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