
# FINAL YEAR PROJECT REPORT

# DESIGN AND SIMULATION OF MIPS PROCESSOR IN HDL VERILOG

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# ABSTRACT

This project deals with the design and simulation of a MIPS processor, which is 32-bit version of the MIPS R2000 processor. The data path of this processor consists of 32, 32-bit registers. In this project we have implemented some of the basic instructions of the MIPS processor such as ADD, AND, SUB, SLT, OR, JUMP, BEQ, SW and LW. These simple instructions are based on only three formats which are R, I and J. The design has a 32 –bit ALU which calculates series of operations according to the instruction format. In order to accomplish this task we used Verilog HDL for designing the modules and the software we used for designing is Xillinx and the other software is ModelSIM that is used for generating the waveforms, that helps us in verifying the right functionality being performed by each and every signal and component we have designed.

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