MCS Project Report

"Hashing in Hardware"

by

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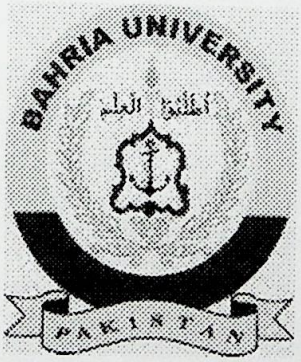

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APPROVALS

We accept the work contained in this report as a confirmation to the required standard for the fulfillment of the MCS degree.

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Introduction

Hardware Description Languages

Digital systems are highly complex. At their most detailed level, they may consist of millions of elements, e.g., transistors or logic gates. For many decades, logic schematics served as the *lingua franca* of logic design, but not any more. Today, hardware complexity has grown to such a degree that a schematic with logic gates is almost useless, as it shows only a web of connectivity and not the functionality of design. Since the 1970s, computer engineers and electrical engineers have moved toward hardware description languages (HDLs). The most prominent HDLs in industry are Verilog and VHDL. Verilog is the top HDL used by over 10,000 designers at such hardware vendors as Sun Microsystems, Apple Computer and Motorola. Industrial designers prefer Verilog. The syntax of Verilog is based on the C language, while the syntax of VHDL is based on Ada. A free Verilog simulator is available from SynaptiCAD, Inc. For Windows 95/NT, Windows 3.1, Macintosh, SunOS and Linux platforms, they offer FREE versions of their VeriWell product, which is available from http://www.syncad.com/ver_down.htm. The free versions are the same as the industrial versions except they are restricted to a maximum of 1000 lines of HDL code.

Verilog HDL

Verilog HDL is a hardware description language used to design and document electronic systems. Verilog HDL allows designers to design at various levels of abstraction. It is the most widely used HDL with a user community of more than 50,000 active designers.
Verilog was invented as simulation language. Use of Verilog for synthesis was a complete afterthought.

The Verilog language provides the digital designer with a means of describing a digital system at a wide range of levels of abstraction, and, at the same time, provides access to computer-aided design tools to aid in the design process at these levels. Verilog allows hardware designers to express their design with behavioral constructs, deferring the details of implementation to a later stage of design in the design. An abstract representation helps the designer explore architectural alternatives through simulations and detect design bottlenecks before detailed design begins.