

Final Thesis
MS –Telecommunication and Networking

Ultra Low Power Small Size RF Transceiver Design for Wireless
Sensor Networks



Written By:
Muhammad Yasir Faheem
(01-244082-050)

Supervised By:
Engr. Dr. Abid Ali Minhas

Department of Graduate Studies and Applied Sciences

Bahria University

ISLAMABAD

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Dated: -----

Final Approval

This is to certify that we have read the thesis submitted by Muhammad Yasir Faheem, Enrollment # 01-244082-050. It is our judgment that this project is of standard to warrant its acceptance by the Bahria University, Islamabad, for the Degree of MS in Telecommunication and Networking.

Project Evaluation Committee

External Examiner: -----

Internal Examiner: -----

Supervisor:
Engr. Dr. Abid Ali Minhas
HOD
Department of Graduate Studies and
Applied Sciences
Bahria University, Islamabad

Dedication

I dedicate this to those who spread peace with help of Islam and those who try to make smile on the faces of poor and needy people and also to my late Grand Father "Ch. Muhammad Ali" (May ALLAH's blessings be always upon him).

A Thesis Submitted To

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As a partial Fulfillment of Requirements for the Award of the
Degree
Of
MS in Telecommunication and Networking

Declaration

I hereby declare that this Thesis “Ultra Low Power Small Size RF Transceiver Design for Wireless Sensor Networks” neither as a whole nor as a part has been copied out from any source. It is further declared that I have done this research with the accompanied report entirely on the basis of my personal efforts, under the dexterous guidance of my teachers especially my supervisor Engr. Dr. Abid Ali Minhas. If any of the system is proved to be copied out of any source or found to be reproduction of any project from any of the training institute or educational institutions, I shall stand by the consequences.

Muhammad Yasir Faheem
Enrollment # 01-244082-050

Acknowledgement

All Praises for Allah the all Mighty Praise be to God (ALLAH), the Cherisher and Sustainer of the Worlds (Rabbul Aalameen), Most Gracious (Al-Rehman), Most Merciful (Al-Raheem) and Master of the Day of Judgment, whose bounteous blessings enable us to pursue and perceive higher ideas of life. He is he, who sent his prophets for the guidance of Human beings and Ginns. Darood and Salaam upon his last prophet, Muhammad (Peace be upon him), his family and his companions, who has the ultimate and eternal way of complete success for this world and the hereafter in the form of Quran: the ultimate manifestation of ALLAH's grace to man, the ultimate wisdom, and the ultimate beauty of expression: in short, the word of God. After this I must mention that it was mainly due to my family's moral and financial support during my entire academic career that enabled me to complete my work dedicatedly. I would like to thanks to my respected teacher's and especially consider it a proud privileged to express my gratitude and deep sense of obligation to my reverend supervisor Engr. Dr. Abid Ali Minhas for his dexterous guidance and kind behavior during my thesis work. I would like to thank my brother, and sisters who encouraged me at those moments when I got exhausted. I also would like to say gratitude to my truly friends especially "the prayer (Nemaaz)" that helped me in every difficulty. I once again would like to admit that I owe all my achievement to my most loving parents who mean most to me, for their prayers are more precious then any treasure on earth. May they all live long with special and unlimited blessing of Allah (Subhana hu Wata'ala).
Ameen Ya Rabbul AaLameen.

Muhammad Yasir Faheem
Enrollment # 01-244082-050

Thesis in Brief

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Undertaken By:	Muhammad Yasir Faheem (01-244082-050)
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ABSTRACT

Wireless Sensor networks are typically used in monitoring the physical or environmental conditions such as motion, vibration, sound, and temperature etc. Typically each sensor node contains a transceiver and some other wireless communication devices. Wireless sensor node operates in the industrial, scientific and medical (ISM) band. Wireless sensor nodes are mostly battery operated and in many applications they are placed un-attended. It is, therefore, required to design both hardware and software that consume very low power during the operations. Current size of the wireless sensor node is of the order of millimeter. Scientists and engineers are trying to reduce its size near to the size of dust particle. This offers a challenge to design wireless sensor nodes that must have small size and consume low power.

Transceiver has a very important role in these wireless sensor nodes, while decreasing size of node, transceiver size to be decreased as well. In this thesis, we have proposed a new transceiver having small size and consuming low power as compare to already ULP915T transceiver. The proposed transceiver contains five blocks namely power amplifier (PA), low noise amplifier (LNA), crystal oscillator (XO), Phase Locked Loop (PLL), and intermediate frequency (IF). The proposed transceiver incorporates less number of LDOs (low-dropout) regulators. The size of transceiver is reduced by decreasing of beneficiary components in such a way that the takes are distributed among all components.

INTRODUCTION

Chapter 1

Introduction

1.1 Technology of WSN

In all types of researches especially in wireless applications dependent nodes the WSN is the area which attracts the attention of researchers because its use is increasing rapidly in all fields which are directly or indirectly related to the human life. These networks need long battery life time and small size with high data rate, so researchers are working on these parameters to make it as small as dust particle.

Wireless sensor network is a combination of some nodes and each node usually comprises in four parts which are microcontroller, antenna, radio frequency transceiver and Memory. WSN technology is now being used in many fields of our daily life such as in roads it is used for traffic monitoring, if we see in the military perspective it is used in controlling army machines (Guns, tanks, etc), so on the other hand it also very useful in health care applications like health monitoring sensing the human temperature etc.

Since, these types of networks like WSN are in the form of small nodes. There are two types of nodes active node and inactive node and these nodes create peer to peer link and multi-hops link depending on commands and the structure of the network, a node is also do broadcasting. Some ways of communication in nodes as shown in Figure 1,

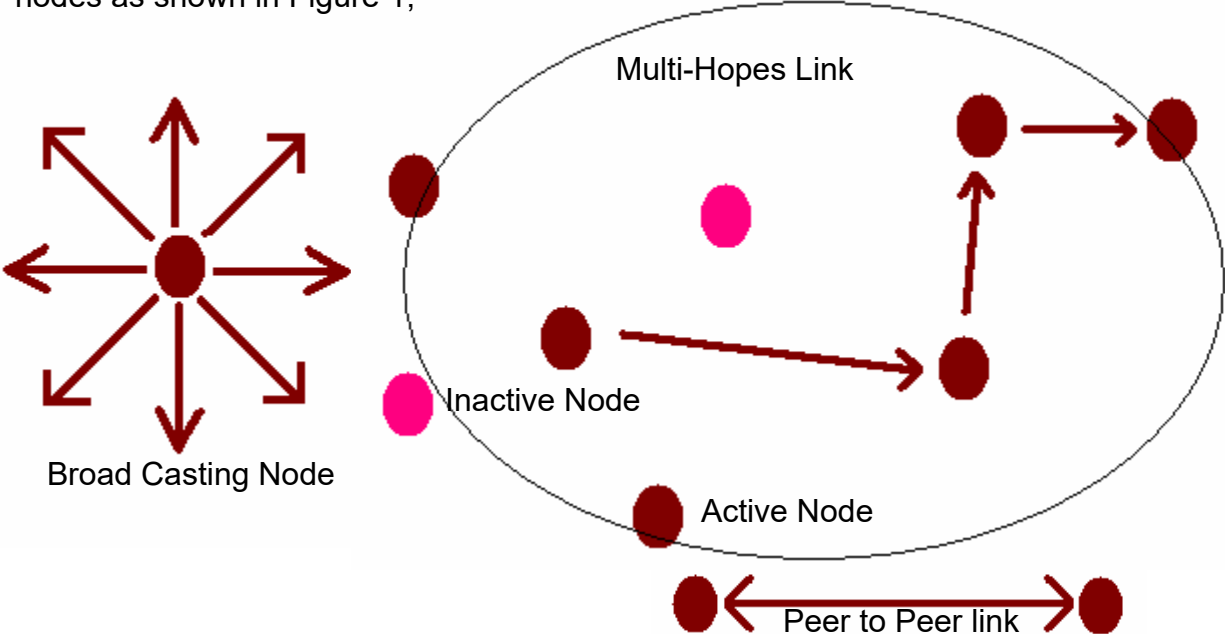


Figure: 1.1 Ways of communication between nodes

1.2 Field of Research

There are two main types of challenges which includes

- **Hardware challenges**
 - This type of challenges includes the miniaturization, energy reduction, power management and hardware security. Hardware security is to protect the sensor node from physically damaged and thieves, it means to protect the hardware physically.
- **Software challenges**
 - Wireless sensor networks deal with the real time world, so in software challenges this real time communication is one of the biggest challenge in all challenges on the other hand privacy and software security is also very important field of research.

1.2.1 Cost

Cost is also a factor which we need to reduce, because the deployment of Wireless sensor networks in large numbers can only be possible if its cost less as much as negligible. Transceiver has a very important role in these wireless sensor nodes, so by making the transceiver less expensive we can reduce the cost of WSN. Single chip transceiver design gives us the low cost solution. In this design we use less number of beneficiary components by giving the same job to other components in a distributed way.

1.2.2 Data Rate and Power of Battery

Data rate and the range of the transceiver or area of access of the node depend upon the power. In some conditions we need both high data rate more range of transceiver but at very less power. There is a tradeoff between data rate and power of the transceiver so we need such a design which can easily solve this problem, in [12] the data rate of transceiver is about 50kbps is maximum at the 1V input, it can be increase and decrease depending upon the design. Because in [5] Alyosha use 3volt input but the data rate is only 20kbps and also in [11] B.P.Otise gives the 40kbps using only 1.2 operating voltage. In [1] R.Van Langevelde gives 45kbps data rate with variable voltage from 1.2v to 1.5v.

Table 1.1 Energy sources and average power for WSN

Energy source	Average Power Density	Usage Life
Lithium cell battery	100 uw/cm ³	One year

Solar cell	10uw/cm3 for indoor and 15 mw/cm2 for outdoor	Very long*
* Depends upon the sun light and place of the solar cell		

1.3 Transceiver Requirements

There are two main sections of transceiver.

- Transmitter
- Receiver

1.3.1 Functions of Transceiver

Transceiver shares the one circuitry for transmitter and receiver

1.3.1.1 Functions of transmitter

Some major Transmitter functions are as follows.

- First it modulates the signal which is base band signal onto Radio Frequency carrier.
- After that it amplify the modulated signal
- Then it provide the matching to antenna to make sure that the power delivery to the free space should be enough efficient to reach its destination.

1.3.1.2 Functions of Receiver

Some major Receiver functions are as follows.

- After receiving the signal from RF carrier it demodulate the base band signal.
- It performs the error correction schemes and extract the original signal from the received signal
- Then it sends it to its desired destination.

1.3.2 Radiated power

We can calculate the minimum radiated power which is needed for two nodes to make communication possible by using following formula.

$$P_{\text{rad, min}} = \{4\pi f/c\} \times \{d^n/G_r G_t\} \times R_{\text{sens}} \times \text{LF} \quad (1.1)$$

Where $P_{\text{rad, min}}$ is the minimum radiated power required for two nodes communication and f is the operating frequency where c is the speed of light 2.99×10^8 , d is the distance between nodes and n is the path loss, G_r is the antenna gain of receiver, G_t Antenna gain of transmitter, R_{sens} is the sensitivity of the receiver and LF is the loss factor.

1.3.3 Efficiency

Efficiency is the major performance parameter of the WSN which also include the better data throughput of transceiver. For better efficiency, transceiver remains active for very long time it depends on the long battery life, so the efficiency also depends on energy per unit time use by transceiver.

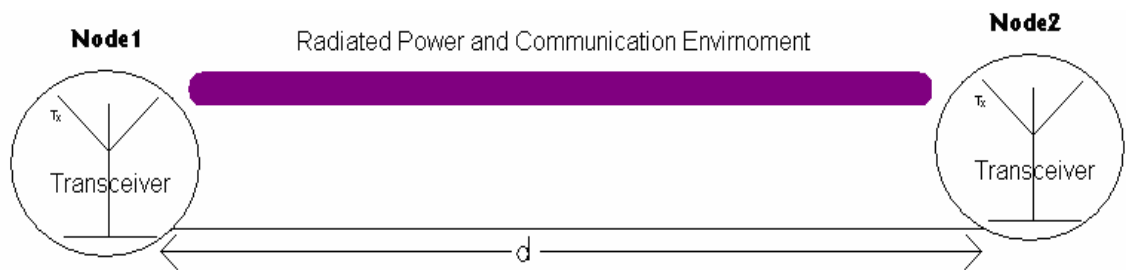


Figure: 1.2 Communication between two nodes transceivers

1.3.4 Modulation schemes for Transceiver

Modulation schemes are use to reduce the cost and to improve the sensitivity of receiver and efficiency of transceiver. (QAM) Quadrature amplitude modulation, Gaussian minimum shift keying (GMSK), Binary phase shift keying (BPSK), Quadrature phase shift keying (QPSK), (FSK) Frequency shift keying, BFSK, and On Off keying (OOK) modulation are the few modulation schemes which are commonly use in the WSN transceiver applications.

1.4 Parts of RF Transceiver

There are usually five blocks of RF transceiver as follows

- Power Amplifier (PA)
- Low Noise Amplifier (LNA)
- Crystal Oscillator (XO)
- Frequency Synthesizer (FS)
- Intermediate Frequency (IF)

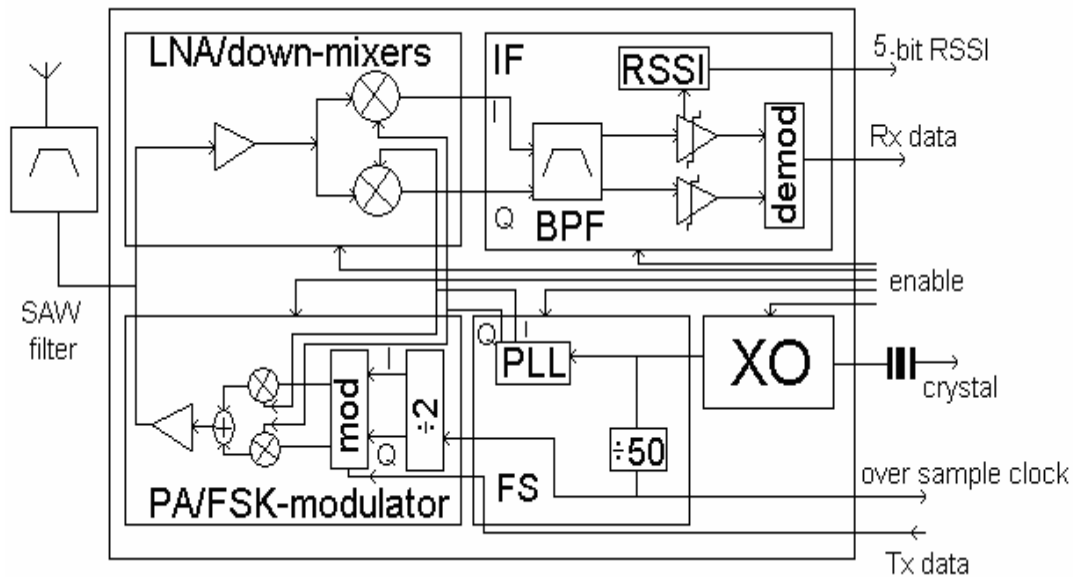


Figure: 1.3 Block diagram of Transceiver parts [1]

The five blocks of RF transceiver are shown in the Figure: 3 which also include the sub blocks of each block. There are five separate enable input provided to five blocks so we can enable each block separately. The terms and their abbreviations are used in the figure as follows

- FSK= Frequency Shift keying
- RSSI=Received Signal Strength indicator
- mod=Modulator
- demod=Demodulator
- BPF=Band Pass Filter
- PLL=Phase Lock Loop
- SAW filter=Surface Acoustic Wave filter
- T_x=Transmitter
- R_x=Receiver

1.4.1 Power Amplifier

PA block contains Power amplifier and FSK modulator. This is the block where transmitter of transceiver gets the data and also after modulating the signal, transmitter amplifies the signal using this block. We also say that this is the transmitter's block because it is on enable state when transceiver in transmitting mode.

To calculate effective output power of the transceiver using power amplifier we used the following formula

$$P_{\text{out.eff}} = V_{\text{out.max}}^2 / 2 \cdot R_{\text{load}}$$

Where $V_{out,max}$ is swing voltage and R_{load} is load impedance which is fixed at 50 Ohm's. So we can only reduce the $V_{out,max}$ to design an efficient PA.

1.4.2 Low Noise Amplifier

LNA enable when transceiver is in receiving mode and LNA is the first part of receiver. Down mixer and LNA are coupled together where down mixer which is quadrature use the double balanced Gilbert cell. Cross coupled amplifier is called Gilbert cell. LNA's input is connected with the out put of PA and SAW filter. In ULP915T when we provide 1.5v to the transceiver using 898uA current the LNA wake up time is less then 20us.

1.4.3 Crystal Oscillator

Crystal oscillator block enables on both time either transceiver is in transmitting mode or in receiving mode. Its job is to provide the reference input frequency to the frequency synthesizer. XO is directly connected to the crystal which is external component of transceiver. Crystal oscillator controlled the amplitude oscillation by which transceiver gets less power consumption. The wake up time of Crystal oscillator is about 1200us applying the 1.5v and its supply current is 18uA.

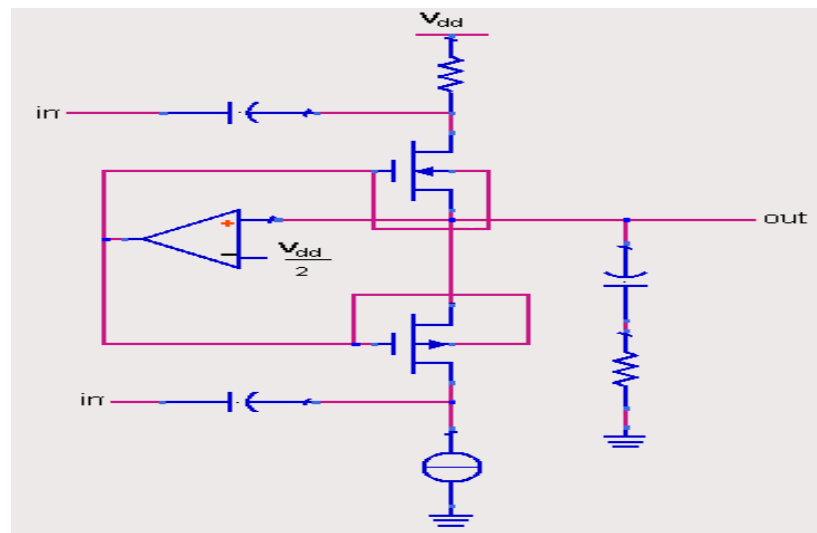


Figure: 1.4 Circuit diagram of LNA [1]

1.4.4 Frequency Synthesizer

Frequency synthesizer also enable in both transmitting and receiving modes. Because frequency is used in both modes, after taking reference frequency from

XO it generates the differential quadrature output signal of higher frequency. Wake up time of frequency synthesizer is less than 20us while supply current is 611uA and voltage is 1.5v in ULP915T. FS block also includes the phase lock loop (PLL) in which (VCO) voltage control oscillator running a twice of frequency I and Q.

1.4.5 Intermediate Frequency

Intermediate Frequency block only enable when transceiver is in receiving mode, so it means that it is the part of receiver. IF block includes band pass filter which is use for channel selection, usually it is 3rd order chebyshev filter and the second part is 5-bit RSSI with limiting amplifier which is consist of five cascaded differential BP amplifier each band pass amplifier generate the one bit of the RSSI signal and the third one is demodulator which is BFSK demodulator as shown in figure 3.

1.5 Types of Transceivers

There are many types of transceivers of many companies but Cisco is the one of the biggest company of the world has the following types of transceivers, which are easily available in the market are shown in below table. Note that transceiver performance with the range perspective depends on the type of communication media which are cables, so its range can be increase or decrease with respect to cable.

Table 1.2 A few types of transceivers which are available in market

Serial Number	Model name	Range
1	WS-G5483	100 meters
2	WS-G5484	550 meters
3	WS-G5486	5 km
4	WS-G5487	70 km
5	GLC-T	100 meters
6	GLC-SX-MM	550 meters
7	GLC-LH-SM	10 km
8	GLC-ZX-SM	70 to 100 km
9	GLC-BX-D	10 km
10	GLC-BX-U	10 km
11	SFP-GE-S	550 km
12	SFP-GE-L	10 km
13	GLC-EX-SMD	40 km
14	SFP-GE-Z	70 km
15	SFP=GE-T	100 meters
16	GLC-FE-100BX-D	10 km

17	GLC-FE-100LX	10 km
18	GLC-FE-100FX	2 km
19	GLC-FE-100BX-U	10 km

1.6 Future of RF Transceiver

RF transceiver is the biggest power consumer among the all parts of the wireless sensor networks. Since it is also very important part of WSN but WSN nodes need large battery timing and long life of work it means nodes do not afford that parts which are higher consumer of energy. So it needs ultra low power transceivers which must be small in size and efficient with respect to energy per unit time. Transceivers are now being used in many technologies like (Wimax) IEEE 802.16, long term evolution (LTE) and in 4G wireless communication the scientists also wants a RF transceiver with multi standard programs which is compactable with different standards at a minimum power consumption. Short range RF transceivers are use in all (ISM) industrial scientific medical band applications. Some applications of RF transceiver which we use in our daily life are as follows

- City Radio
- Walkie-talkie
- Mobile phone
- Digital TV

Scientists are going to build a transceiver in your personal computers for satellite communication in near future.

LITERATURE SURVEY

Chapter 2

Literature survey

2.1 Initial work

In [1] R.Van Langevelede has given the “An ultra low power 868/915 MHz RF transceiver for WSN Applications” solution which has fabricated in 0.13um technology. Author has used binary FSK modulation scheme and the data rate of the transceiver has been 45kb/s where the supply voltage has been 1.2V to 1.5V. Author has minimized the size of chip by dropping some internal components like inductors and has given the small size solution. The following table shows the measurements of transceiver.

Table 2.1 Measurements of transceiver performance [1]

Modes	Parameter	Value	Unit
General	Operating frequency	862/915	MHz
	Data rate	45	Kb/s
	Frequency deviation	181/190	KHz
	Chip area	1.5	mm ²
	CMOS technology	0.13	um
	External components	4	.
	Supply voltage	1.2/1.5	V
	Sleep current	0.8	uA
Receive mode	Supply current	1.6	mA
	Sensitivity at BER 0.1%	-89	dBm
	Max input signal	-10	dBm
	LO leakage	-90	dBm
Transmit mode	Supply current	1.8	mA
	Output power	-6	dBm

R.Van Langevelede has solved three problems for RF transceiver but data rate has been not very high and some extra components also still in the transceiver design like, five LDO's (low drop out regulator) instead of one have used. Another problem also there like now most of transceiver need to operate at 2.4GHz frequency because this operating frequency is rapidly used in all communication systems [1].

Chinung-An Chen et al .In [2] have given the 2.4GHz transceiver solution for bio medical applications like health care monitoring using four level hierarchy systems with the help of pipeline and mapping application of wireless sensor network. This architecture reconfigures the map applications of WSN system. Authors have used the adaptive low power system design that reduces the power consumption, where the maximum distance of transmission has been 10 meter. The transmitted power can be calculated using following formula

$$P_t = - G_r - G_t + \text{Path Loss} + P_r \quad (2.1)$$

Where path loss can be calculated as below

$$\text{Path Loss (dB)} = 32.44 + 20 \log F_{\text{MHZ}} + 20 \log D_{\text{km}} \quad (2.2)$$

In equation (3.1) P_t P_r G_r and G_t have been transmitted power, received power, receiver gain and transmitter gain respectively. But the data rate has been 40Kb/s which is not too much high in bio medical field we need high data rate and more accuracy as compare to other communication fields so we need a design that can control the whole WSN system with less power high data rate using better accuracy and more sensitive on the human temperature perspective [2].

Author has used preamble sampling MAC (Medium Access) protocol to reduce power consumption of wireless sensor networks and embed it on low cost CC2420 chip con while IEEE standard has been 802.15.4 for transceiver in [3]. The supply voltage has been 1.8V to 3.3V where the operating frequency has been 2.4 GHz for the transceiver. After synchronization first time it takes a lot of time to detect the preamble that has been a waste of time and energy then, Wise MAC has been used to solve this problem which reduce the detection time but dew to the drift between clocks it came on the un synchronization state that has another problem then J.J Perez has given the “preamble sampling technique” in which CC2420 chip has been used to send useful information instead of wasted preambles using acknowledgment frame from both sides. Which also decrease the power consumption, the time and data transmission diagram shows as below in figure 3.1.

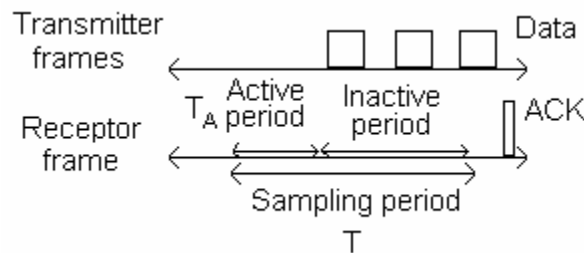


Figure: 2.1 Using MAC protocol timing diagram of transmitter and Receptor frames [3]

Where T , ACK, T_A are sampling time, acknowledgment frame, active period duration respectively. In figure it has been clearly seen that first ACK frame received then transmitter send new frame if ACK frame not reach its destination then transmitter can not be able to send new frame [3], where on reception side if ACK frame has not reached on this side then after some time it has gone to its inactive state during sampling time. This is the big problem it must send negative ACK frame to solve this problem.

In [4] Chi-Jeon Hwang has used OOK (On-Off keying) and “quasi-Monolithic Microwave Integrated Circuits (quasi=MMICs)” method for Radio Frequency transceiver. In health monitoring sensitivity has been a big problem which has related to the low operating voltage, using OOK modulation author has solved this problem (fabricated on GaAs substrate). There have been two states on state and off state in off state the power consumption has been less then $5\mu\text{W}$ and LNA supply voltage has been 0.3V where envelop detector supply voltage has been 0.9V and the operating voltage of transceiver has been 1.2V . The block diagram of proposed solution as follows.

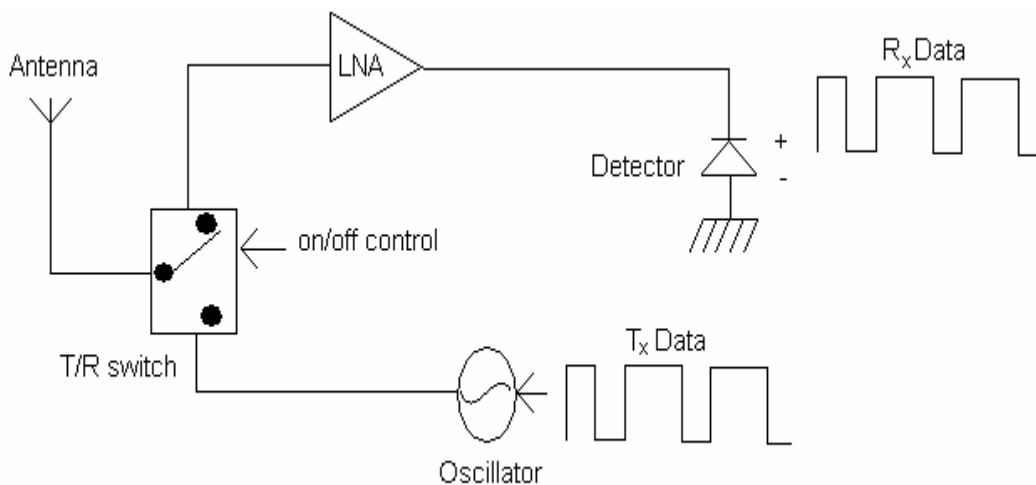


Figure: 2.2 Block diagram of proposed RF transceiver [4]

Where T/R switch has been the transmitter/receiver switch, using on/off keying at a time the transceiver either in transmitted mode or in receiving mode. The data rate 10kbps has been very low and synchronization time has not very small.

In [5] Alyosha Molnar has used $0.25\mu\text{m}$ CMOS technology for RF transceiver. In WSN system the communicating range of the transceiver has been very important factor. Authors have needed long battery life cell one chip solution and all functionality of transceiver in very less cost. There have been two techniques which can minimize the cost and power consumption of the transceiver. The first one has been stacking system in such a way that multiple circuits stack in a single bias circuit it means Author has reused the bias current. Second one has been single high quality inductance for resonant core of the oscillator and drives

all circuit through the core of oscillator. But it operates on 3 volts supply, which has been very high supply voltage in this field. Author has locked digital FLL (Frequency Lock Loop) to the Radio frequency oscillator to reduce the power consumption, where all bias current has been programmable and inter-mediate frequency has been programmable on 1.75MHz to 100 KHz. Finally author has obtained the 16 meter range of the transceiver from both ends and in transmit mode it has consumed the 1.3mW power and in receiving mode it consume about 1.2mW power. Still the data rate has been very low about 20 Kb/s. Note that the above range was only for indoor communication and the both chips were in bias state [5].

In [6] shih-Lun Chen research work has been on WBSN “Wireless Body Sensor Network” which has been commonly used in all healthcare applications. Author has found that during ECG “electrocardiogram” of human the sensitivity of temperature has been very important factor and with the existence of the body temperature it has needed to make a low power thermal sensor nodes for healthcare applications. WBSN consist of four layer system architecture structures which have been system layers, Application layer, sensor group layer and sensor layer. This layered architecture helps the WBSN system in development and verification fields. The voronoi diagram to explain the sensor network according to cells and “adaptive low power design” to solve above problem in which Author design pipeline methodology for controlling each layer has been used, but it increase the complexity then to solve this problem then author has used a communication cycle in such a way that first WBSN system synchronize using digital clock with the sensor nodes in time sharing protocol then in less time the communication starts between nodes [6]. At the end Authors got that for 240 electrocardiogram signals per second the power consumption has 106.3 μ W to 220.4 μ W. Since in shorter communication range systems the range of transceiver not a very important but less power consumption and high data rate matter a lot.

Y.H.Chee and A.M.Niknejad [7] have given idea about injection locked transmitter for WSN utilizing FBAR (Film Bulk Acoustic Resonator) for transmitter. Authors have used 0.13 μ m CMOS technology for transmitter design. The efficiency of the transmitter has been very low about 19% in pervious researches so Author wants to increase the efficiency of the transmitter using injection locked system and proposed that injection locked system has a self control system and it automatically minimize the load on its all driver. Also Authors have replaced the power amplifier with the efficient power oscillator to improve the power efficiency of the transmitter. Authors have needed the FBAR (which consume the 90 μ W power) to obtained the stable 1.9 GHz carrier frequency. After all implementations Authors have been able to improve the efficiency up to 32% with the 50Kb/s data rate using 50% on-off keying. Transmitter consumes 1.6mW power. The operating frequency not in the ISM band the designed transmitter should also be able to operate in 2.4GHz.

In [8] the researchers have done work on “wake up frame scheme” for transceiver, Authors have used wake up frame scheme on the place of wake up preamble scheme. The problem has that, at the time of preamble sampling wake-up preamble scheme takes more time because it sample the preambles periodically after every cycle so a long wake up time for transceiver and more power consume on wake-up time. In order to reduce the wake-up time and power consumption of the transceiver Author has used the wake up frame scheme. Another scheme, if a node wants to communicate with a sleeping transceiver it send the wake up signal which made the transceiver in a communicating mode that has called wake up signal scheme which has not been efficient scheme [8]. So in proposed solution Author has used FPGA switches in which transmitter send a data frame for a long wake up, after detecting preamble FPGA switches turned on and it converts transceiver into receiving mode and it began to receive the frames. On sleeping mode the power used by transceiver has 27 μ W. Where on working time it has been used 27mW power, FPGA has used 20mW in active mode and 1.5 μ W in standby mode. Microcontroller of the node use 33mW and 90 μ W for active mode and sleeping mode respectively. Although the power consumption has been less due to above method but synchronization time not very small due to the use of preamble scheme.

Ben W.Cook and Axel Berny [9] have designed a passive front end for transceiver in mesh networks. Authors have used 0.13 μ m CMOS technology for fabrication. The problem has been power consumption and overall efficiency of the transceiver; authors have used “integrated resonant matching network” to achieve above goals. Researcher has made a comparison between matching network and passive mixer network. After implementing passive mixer authors have improved the overall efficiency up to 30% and power amplifier efficiency up to 45%, authors have received some other results which are in below table.

Table 2.2 Summary of measured results [9]

Parts	Fields	Minimum	maximum
Overall	Supply voltage	360mV	600mV
	Binary FSK deviation	300KHz	1000KHz
Receiver	Power consumption	200 μ W	750 μ W
	Noise figure	5.11dB	11.8dB
Transmitter	Power consumption	700 μ W	1120 μ W
	Output power	140 μ W	320 μ W
Voltage control oscillator	Power consumption	160 μ W	700 μ W
	Frequency	1.95GHz	2.38GHz

Usually the mesh circuits have a complex circuitry and it creates difficulties to solve hardware problems in transceiver.

In [10] the Author has done the research in two key issues which have contained cost and power dissipation issues. Vineet Sahula has described that complexity in the implementation of the transceiver made the chip very expensive. Author has given the solution using HCFG “hierarchical concurrent flow graph” design approach. If the time of completing the design of chip has reduced then the cost of chip automatically has reduced. [10] A tool which examines the time duration of a complete design process has designed. Author has analyzed that in large complex system design HCFG approach has been a best solution. But there has not been temperature controlled method in the above research which has been a very important factor in wireless mobile transceiver field.

B.P Otis and Y.H.Chee [11] have designed a two channel transceiver which has been MEMS “Micro Electro Mechanical System” based. Authors have used RF-MEMS resonator. The problem in which Authors have focused were turn on time of transceiver and power dissipation of the transceiver. Authors have reduced the over head of a duty cycle and used two inductors of 1.2nH and 8nH, where on the other side, FBAR has used to obtain 1.9GHz frequency and implement transceiver on 0.31 μ m CMOS technology chip [11]. Authors have reduced the turn on time and made it equal to the 10 μ s therefore the efficiency increase of the transceiver up to 17%. Where the supply voltage has been 1.2V and current which transceiver consumes has been 3mA. There has no external component in their design. It has been designed for MEMS technology and this technology commonly used on 2.4GHz systems so to make transceiver compatible with other technologies it must be designed on 2.4GHz operating frequency.

In [12] the researchers have been narrow down their research on a power consumption of a transceiver for WBSN “Wireless Body Sensor Network” applications. In this research Authors have used “Zinc-air coin cell” with printed battery technologies. The supply voltage has been 1V and the data rate was 50Kbps, where the CMOS technology has been 0.31 μ m [12]. This work has been only effective for biotelemetry applications.

In [17] Authors have designed a “Fully Integrated 2.4-GHz CMOS RF Transceiver for IEEE 802.15.4” The problems in which Authors have focused the research were 1/f noise and I/Q mismatch and some other like linear power and the DC offset. Authors have proposed the dual conversion architecture for above problems and Trans-conductance linearization technique using a mixer which has based on current mirror amplifier [17]. Using 0.18 μ m CMOS technology Authors have obtained 8dB noise figure for receiver, where supply voltage has been 1.8V and transmitter current consumption has been 15mA and when transceiver has been in receiving mode then current consumption has been 9mA. Power consumption of transmitting mode and receiving mode has been 31mW

and 45mW respectively. This work has been only applicable on WPAN “wireless personal area network”.

Researchers have fabricated a MMIC “Monolithic Microwave Integrated Circuits” based transceiver [18]. Low cost, low input voltages have the key issues in this research, multifunction transceiver also needed for the wireless applications. Authors have used the SAGFETs “self-aligned gate field effect transistor” to make transceiver less expensive. Authors have used TDMA “time division multiple access” for transmit, receive, and sleep modes. After implementation [18], as there has been used high integration for transceivers design therefore the area has been $1.5 \times 2.5 \text{mm}^2$. Where the supply voltage has been 2.2V and the efficiency of transmitting signals has been 26%. In transmit mode transceiver has utilized 196.5mA and in receiving mode it has consumed 3.1mA current. Since the operating voltage has been very high as compare to days development.

In [19] L.H.Crockett and N.C.MacEwen have needed an ultra ad-hoc technology for wireless network which also based on low power supply voltage. Authors have used OOK modulation which has the simplest modulation scheme. But the data rate has very low about 10Kbps. Because Authors have designed the digital transceiver so Manchester coding scheme has been used this helped in decreasing the over head of synchronization. Transceiver has used 11000 gates [19]. Authors have used half sine pulse shaping to decode the Manchester encoding scheme but that has not been work efficiently for this purpose. But the SNR dew to this method has increased up to 2.38dB.

In [20] Authors have worked on low power because all applications of wireless communication highly required low power transceiver. The issues has discussed in this research work have contained low cost and battery life time. Authors have highlighted the tradeoff between performance and power consumption of a transceiver. Using $0.51 \mu\text{m}$ CMOS technology it has replaced the unbalanced structure with differential one using same chip in this research. Then the balanced structure has given the better power consumption [20]. It also been added some passive components in transceiver like discrete external inductors; Authors have not been adding on-off chip inductors because it has utilized more power of the chip. The supply voltage of the transceiver has been 1V where total power consumption of the transceiver has been 1mW. The operating frequency has been 2.4GHz. But the fabrication technology has not been latest as to day’s requirement.

Xin Liu and Myint Wai Phyu have given the IC base band transceiver design in $0.18 \mu\text{m}$ CMOS technology for wireless body area networks (WBAN) in which Authors have optimized the performance of the transceiver [21]. In this field miniaturization has the major issue which has also related with the power consumption of the transceiver. Authors have wanted to increase the battery life time of transceiver, so it has proposed physical layer architecture which reduced the power consumption of the transceiver and also transceiver performance

increased in all short range communication in this research. Physical layer graphical representation has shown as below.

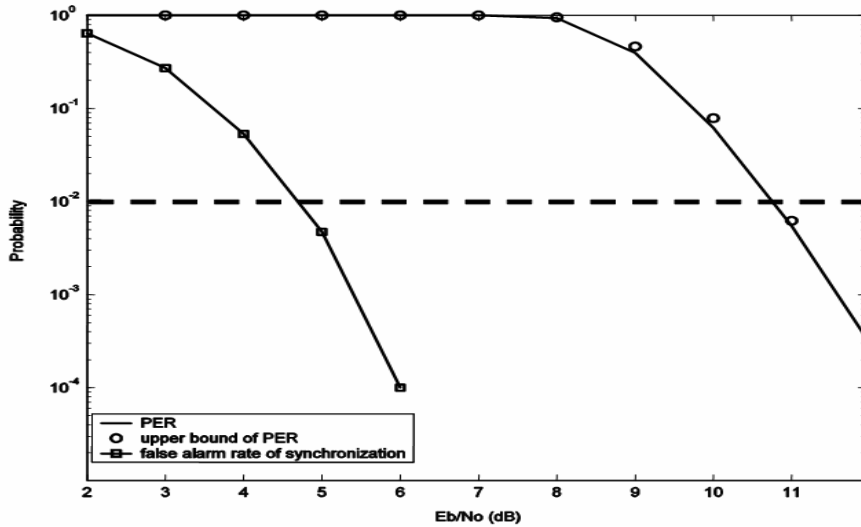


Figure: 2.3 Performance of physical layer in worst condition [21]

Transceiver has consumed 240.24 μ W and 202.34 μ W power on transmitting and receiving modes respectively [21]. After implementation Authors have got very low power transceiver IC chip. But data rate very low as compare to the existing researches.

In [22] Researchers have designed a very low power wearable transceiver for medical specialist. There has been no such a low power transceiver which has also been wearable in previous researches, like there has been minimum 9V operating transceiver before this work, to solve that problem Authors have proposed a very low power wearable transceiver design. So Authors have used an efficient wireless communication scheme which has used the human body as a transmission medium [22]. Authors have fabricated the transceiver chip on 0.18 μ m CMOS technology which able to achieve up to 15Mbps data rate. Authors have used Cadence simulator for circuit simulation. The supply voltage has been 1.8V and range of transceiver has been 2 meter. Where carrier frequency has been 1-20MHz and power consumption has been 5mW of the transceiver. But since in health care medical applications a real time communication plays a vital role so to over come this problem we have to need to do work on real time bio sensor networks.

Andrea Morici and Saul Rodriguez [23] have given a front end design of a receiver for wireless sensor networks using 90nm CMOS technology. The smart device and low cost has the performance parameters. There has been no inductor in LNA (low noise amplifier) in their design. Authors have used nanometer technology to increases the performance of transceiver. Authors have proposed a design for balun integration in low noise amplifier of the receiver,

where balun is device which tunes the LNA on the working frequency of 2.4GHz. This device composed of coils [23]. Authors have used that load, which has completely resistive in their design. After implementation the power consumption of receiver front end has been 3.6mW where the voltage supply has been 1.2V and the power gain has been 21.8dB. The use of 90nm fabrication technology covers more area and size of receiver increased.

2.2 Summary of Literature Survey

In all [1], [2], [3], [4], [5], [7], [8], [9], [10], [11] the size of chip is 0.13 μ m. And the voltage was used 1.2 volt, 1.5volt and the minimum 1 volt was used in [12]. 50 ohm's load was also fixed in all above papers and binary FSK (frequency shift keying) was used with data rate of 50kbits/s and in some papers 45kbits/s. Commonly all transceivers were operating on industrial, scientific and medical (ISM) band. In all previous researches there were limitations like if power consumption has decreased then data rate has not been much high and if supply voltage has decreased then range of transceiver has also been minimized so there have been many such kind of trade offs which make the research limited. But still there have been a lot of issues which wants the attention of researcher in wireless communication networks either it have WSN, WBSN, WBAN or any other. We can only use CMOS technology for transceiver fabrication; there has been no any other technology which has best suitable for such a low power and small size transceivers.

2.3 Road to proposed solutions

From 1975 to 2010 the supply voltage decrease in every proposed solution and in future you will see more improvement. The graph between supply voltage and years is shown in below figure 4.5. Where solid lines represents the upper limit of supply voltage and dashed lines represents lower limit of the voltage in figure 4.5

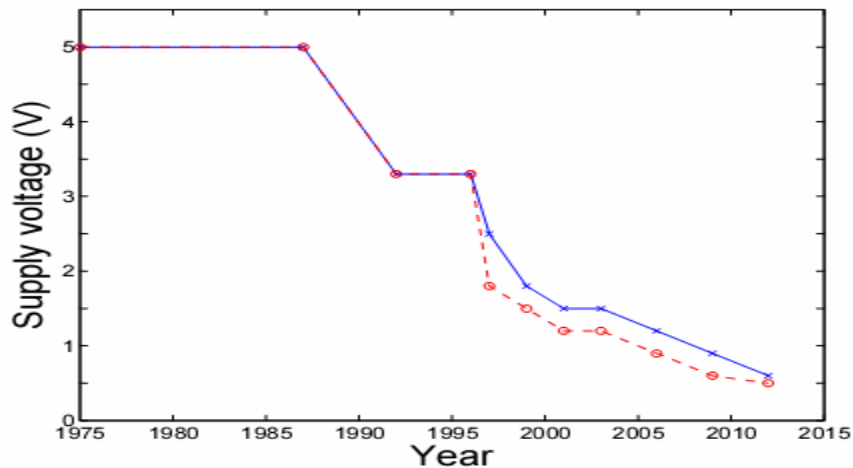


Figure: 2.4 Decrement in supply voltage year by year using proposed solutions [24]

Another figure shown below which gives us the graph between size of chip and years and tell how the size of chip minimized year by year.

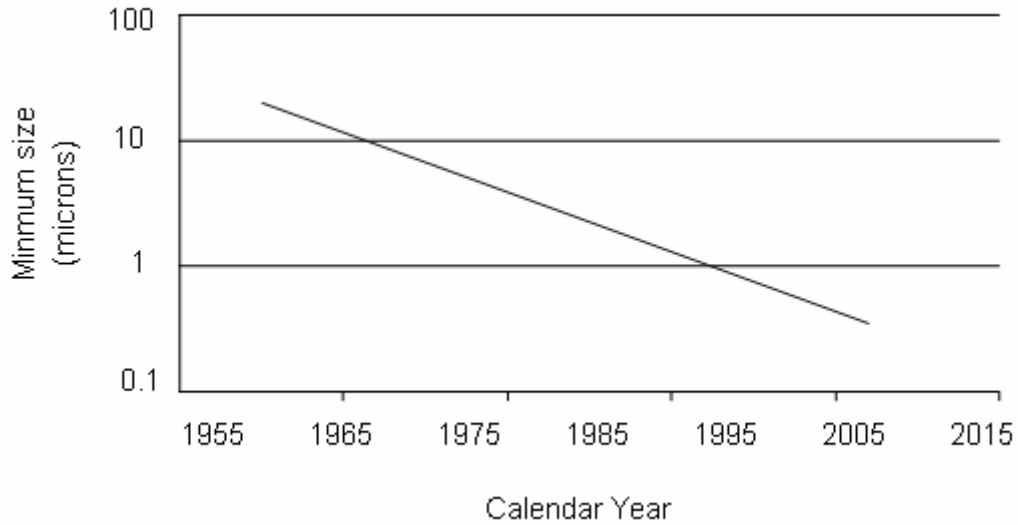


Figure: 2.5 Average minimum size of a chip year by year [25]

There are also numbers of components which are increasing year by year on the same size of chip like transistor as shown in below figure.

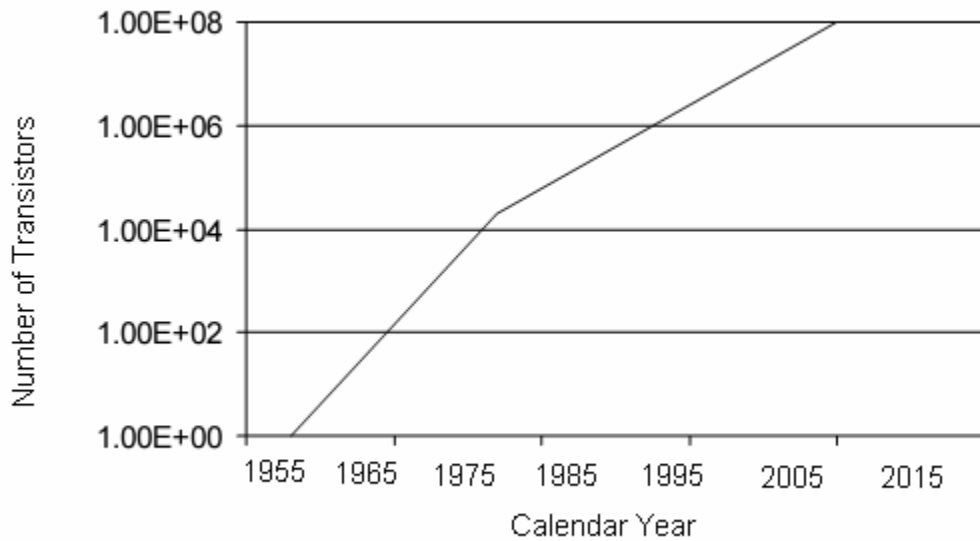


Figure: 2.6 Increase in number of transistor in chip year by year [25]

Table: 2.3 Measurements of some reference researches

Reference papers	Operating frequency	Operating voltage (V=volt)	Chip area (mm ²)	CMOS Technology (μm)	Power Consumptions	Type of application	Sensitivity (dBm)	Eb/ No (dB)	Data Rate Kbps
R. van Langevelde, 2009,[1]	868MHz	1.5V	1.5	0.13	N/A	WSN	-89	N/A	45
Chiung-An Che,2007[2]	2.4GHz	1.8V	4.5	0.18	3.47mW for PA And 3.45mW for LNA	WSN bio-medical	-74	For BER=10 ⁻⁵ is 14	40
Chi-Jeon Hwang, 2009 [4]	10GHz	1.2V	50μm ²	N/A	0.9mW	WSN	N/A	N/A	10
Alyosha Molnar 2004, [5]	900MHz	3V	1.6	0.25	1.3mW	WSN	-94	N/A	20
Shih-Lun Chen, 2009,[6]	2.4GHz	1.8V	4.5	0.18	106.3μW or 220.4μW	WBSN biometrics and healthcare	-74	For BER=10 ⁻⁵ is 14	40
Y. H. Chee, 2005 [7]	1.9GHz	280mV only for transmitter	N/A	0.13	1mW for transmitter	WSN	N/A	N/A	50
Ben W. Cook, 2006 [9]	2.4GHz	400mV	2.1	0.13	750μW for receive mode and 1120μW for transmit mode	WSN	N/A	N/A	N/A
B.P. Otis, 2004[11]	1.9GHz	1.2V	8	0.13	N/A	WSN	-78	N/A	40
A. C. W. Wong, 2007[12]	868MHz	1.5V	7	0.13	2092μA for receive mode and 2368μA for transmit mode	Wireless Bio-telemetry	-102	For BER=10 ⁻³ is 47	50
Lckjin Kwon [17]	2.4GHz	1.8V	13.32	0.18	31mW in receive mode and 42mW in transmit mode	WPAN	N/A	N/A	N/A
Alain-Serge Porret, 2000 [20]	434MHz	1V	N/A	0.5	100μW	Health monitoring	-94	N/A	24
Xin Liu, 2008 [20]	N/A	1.8V	3.24	0.18	202.3μW in receive mode and 240.2μW in transmit mode	WBAN	N/A	For BER=10 ⁻⁴ is 11	N/A
Jin Huang, 2009 [22]	20MHz	1.8V	0.56	0.18	5mW	Human body communication	-30	N/A	15Mbps
Andrea Morici, 2009 [23]	2.4GHz	1.2V	0.12	90nm	3.6mW	WSN	-85	N/A	N/A

PROBLEM STATEMENT

Chapter 3

Problem statement

3.1 Problem statement

A wireless sensor network is comprised on nodes. Each wireless sensor node is operated by the batteries. To extend the life of node it's important to have energy efficient transceiver design because RF transceiver is the biggest consumer of energy in WSN. We need such a design which gives us simple, reliable, less cost, low power and small size solution for RF transceiver in low operating voltage and must operate in 2.4GHz frequency (ISM band) to make its use common in all fields of life.

3.2 Objectives

In the field of wireless sensor network, the RF transceiver design needs the attention of researchers from many aspects but my research focused on two parameters. The first one is its size and the second one is its power utilization. In this thesis following five objectives are achieved.

1. The size of RF transceiver chip is reduced.
2. The operating voltage (input) is reduced from 1.5 to 1 volt without effect on output voltage means giving maximum output at transmitter end.
3. The energy per unit time of the RF transceiver is reduced.
4. The cost of chip is minimized.
5. The transceiver circuitry is made simple.

PROPOSED SOLUTION

Chapter 4

Proposed solution

4.1 Proposed Solution

We propose an Ultra Low power 2.4 GHz small size RF transceiver (ULP2.4T) that is of small size and consuming low power. The proposed chip contains five blocks which are power amplifier (PA), low noise amplifier (LNA), crystal oscillator, PLL, and IF.

In ULP915T, high voltage is converted to low voltage by using five low-dropout (LDO) regulators. We propose three low-dropout (LDO) regulators to achieve the same function by changing the circuit configuration. In the first part of the solution, we use only one LDO for two blocks. As second part of the proposed solution, we have removed the inductors which are present in the ULP915T. Third part of proposed solution takes only three enable pins instead of five in the circuit as taken in ULP915T. When the transceiver is in transmitting mode, then two pins En1 and En2 are enabled. One enable pin En1 is connected with Power Amplifier and other enable pin En2 is connected with PLL and Crystal Oscillator. When transceiver is in receiving mode then pin En3 is enabled and pins En1 and En2 are disabled. Less number of pins connections consequently occupies less space, thus the size of chip is automatically reduced. It also improves the power efficiency of the transceiver, which is one of the major performance parameters of the proposed low power transceiver. Since ULP2.4T is designed to operate in 2.4 GHz, therefore, reference frequency of 50 MHz is chosen.

The block diagram of proposed transceiver is depicted below.

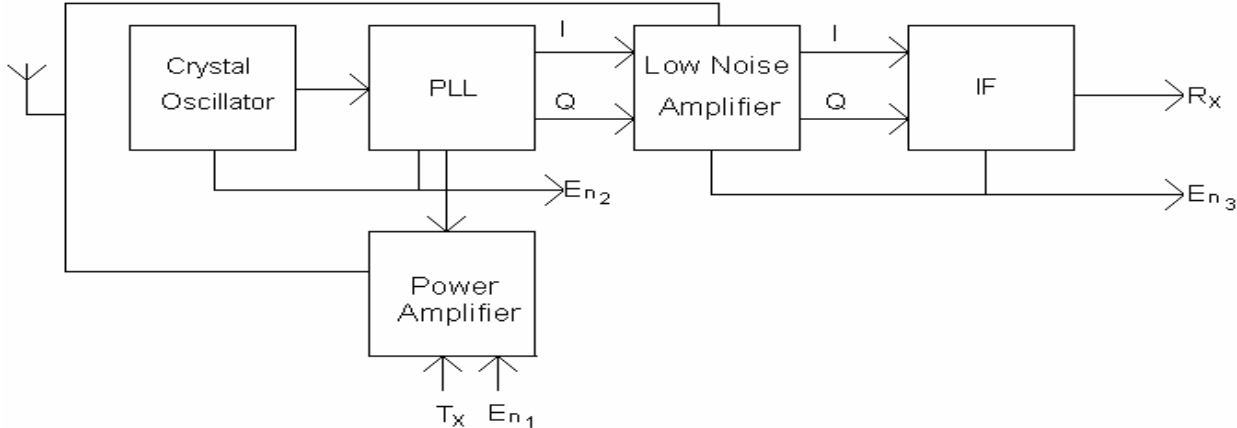


Figure: 4.1 Block diagram of proposed transceiver

Where PLL is Phase Locked Loop and IF stands for Intermediate Frequency which includes demodulator and band pass filter blocks. R_x is receiving end side and T_x is transmitting end side. En1, En2 and En3 are pins that might be enabled or disabled. We need to reduce the number of components in the RF transceiver in such a way that the whole transceiver must perform exactly in right way and give the true expected output. Now we describe one by one the factors which are improved using our proposed solution.

4.2 Performance parameters/ Research Variables

Since it is described earlier in last chapter that in transceiver design there are certain parameters which are related to each other for example; output power is directly proportional to the range of the transceiver. In low power transceiver design wireless sensor node needs low operating voltage and maximum range for a transceiver.

There are some performance parameters considered during with low power and low cost transceiver.

- Data rate
- BER(bit error rate)
- Synchronization
- Simplicity
- Low cost
- Low power
- Miniaturization
- Radio range

There is also another important factor time; this includes sleeping time, wake time and standby time headings. If researchers consider each and every factor in positive way by forgetting that how much it takes effect on the output then at the end researchers will get the efficient and reliable transceiver, because small improvement in each factor of research will give them a big improvement in whole research.

There are some components which are indirectly effect on the performance of the transceiver for example antenna, crystal and external filter.

4.2.1 Power Dissipation

Since our transceiver is designed to work in the range of 1.2V to 1V as operating voltage instead of 1.5V, therefore, power dissipation will be less. We have introduced a converter to convert 1.5V into 1.2V. This helps to use one LDO instead of five for all blocks as shown in below figure 5.2

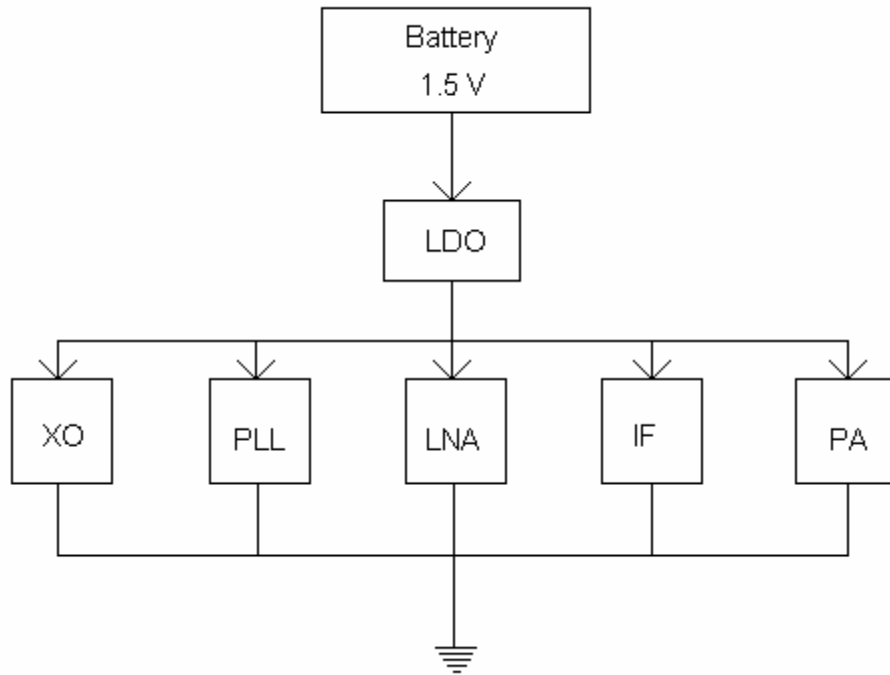


Figure: 4.2 Conceptual block diagram of operating voltage in proposed solution

4.2.2 Cost

Cost is the second important factor of any device. Cost is automatically reduced when we reduce the chip area by using less number of enable pins and less number of voltage converter components in the chip.

4.2.3 Miniaturization

Scientists are always trying to reduce the size of transceiver and we have tried the same in this thesis. We have achieved this by reducing the number of blocks by keeping the functionality same. We have also reduced the number of connections by using the concept of distributed working. This is explained in figure 4.3



Figure: 4.3 Removal of two pins in our proposed solution conceptual view

If A_{P_3} is the area of three pins and A_{P_5} is the area of five pins, then

$$A_{p3} < A_{p5} \quad (4.1)$$

Thus the size of transceiver should be minimized. Now we see miniaturization due to second idea as shown below,

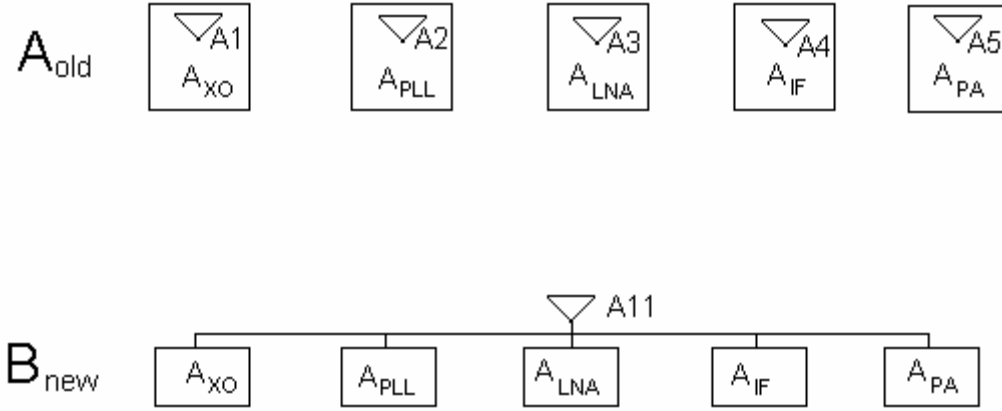


Figure: 4.4 Comparison between ULP915T and ULP2.4T with respect to Area

Where A_{old} shows the view of ULP915T and B_{new} shows the view of ULP2.4T with respect to area. The following equations govern the area calculations:

If

$$A_{11} = A_1 = A_2 = A_3 = A_4 = A_5 \quad (4.2)$$

Then

$$(A_{XO} + A_1) + (A_{PLL} + A_2) + (A_{LNA} + A_3) + (A_{IF} + A_4) + (A_{PA} + A_5) = A_{tot} \quad (4.3)$$

$$(A_{XO} - A_1) + (A_{PLL} - A_2) + (A_{LNA} - A_3) + (A_{IF} - A_4) + (A_{PA} - A_5) + A_{11} = A_{tot\ new} \quad (4.4)$$

Such that

$$A_{tot\ new} < A_{tot} \quad (4.5)$$

A_{tot} is the total area in ULP915T and $A_{tot\ new}$ is the total area of ULP2.4T. Where A_{XO} , A_{PLL} , A_{LNA} , A_{IF} , A_{PA} are the areas of crystal oscillator, phase locked loop, low noise amplifier, intermediate frequency and power amplifier respectively and A_{11} , A_1 , A_2 , A_3 , A_4 , A_5 are the areas of voltage converter circuitries.

Implementation and Simulation Details

Chapter 5

Implementation and Simulation Details

5.1 Implementation and Simulation of Transceiver Circuits

The implementation of five blocks which we designed for ULP2.4T is shown in figures 5.10, 5.11, 5.12, 5.13, and 5.14. These blocks are simulated initially separately to verify the required outputs for certain designed inputs. Afterwards these blocks are combined to have a full transceiver circuit and again simulation is performed. The results are discussed in next chapter.

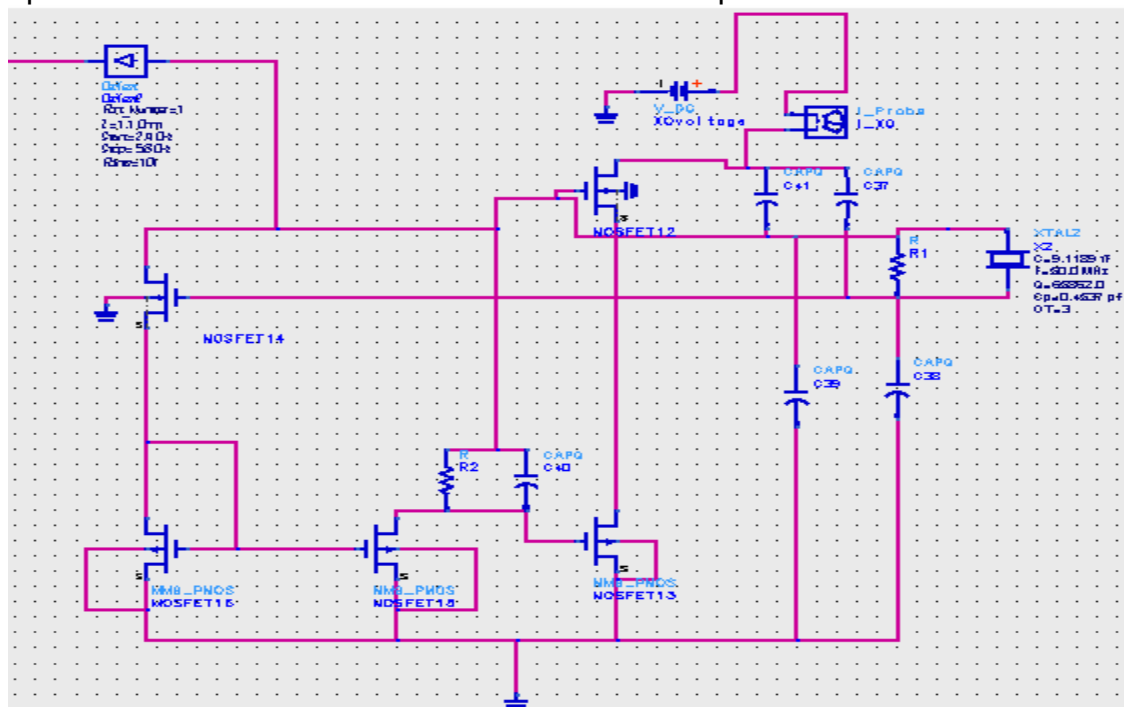


Figure: 5.1 Layout of low power crystal oscillator

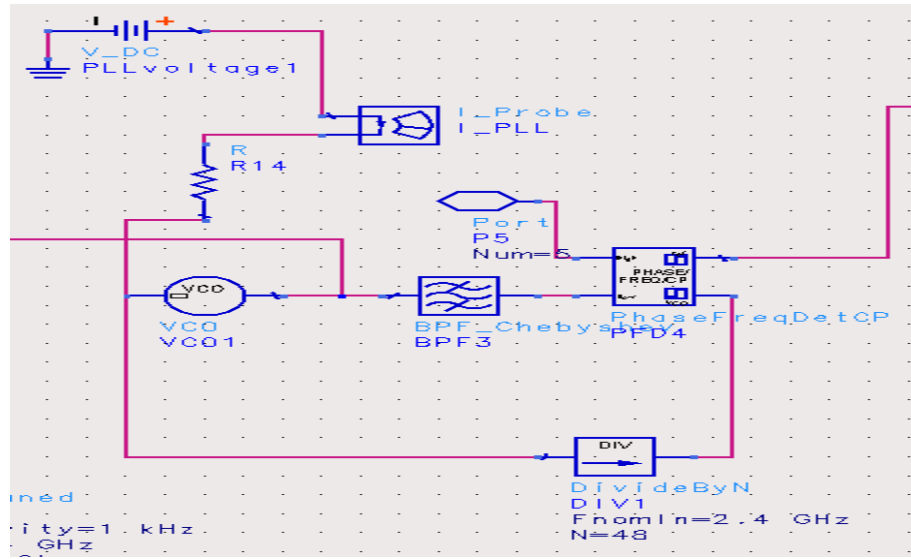


Figure: 5.2 Layout of Phase Locked Loop (PLL)

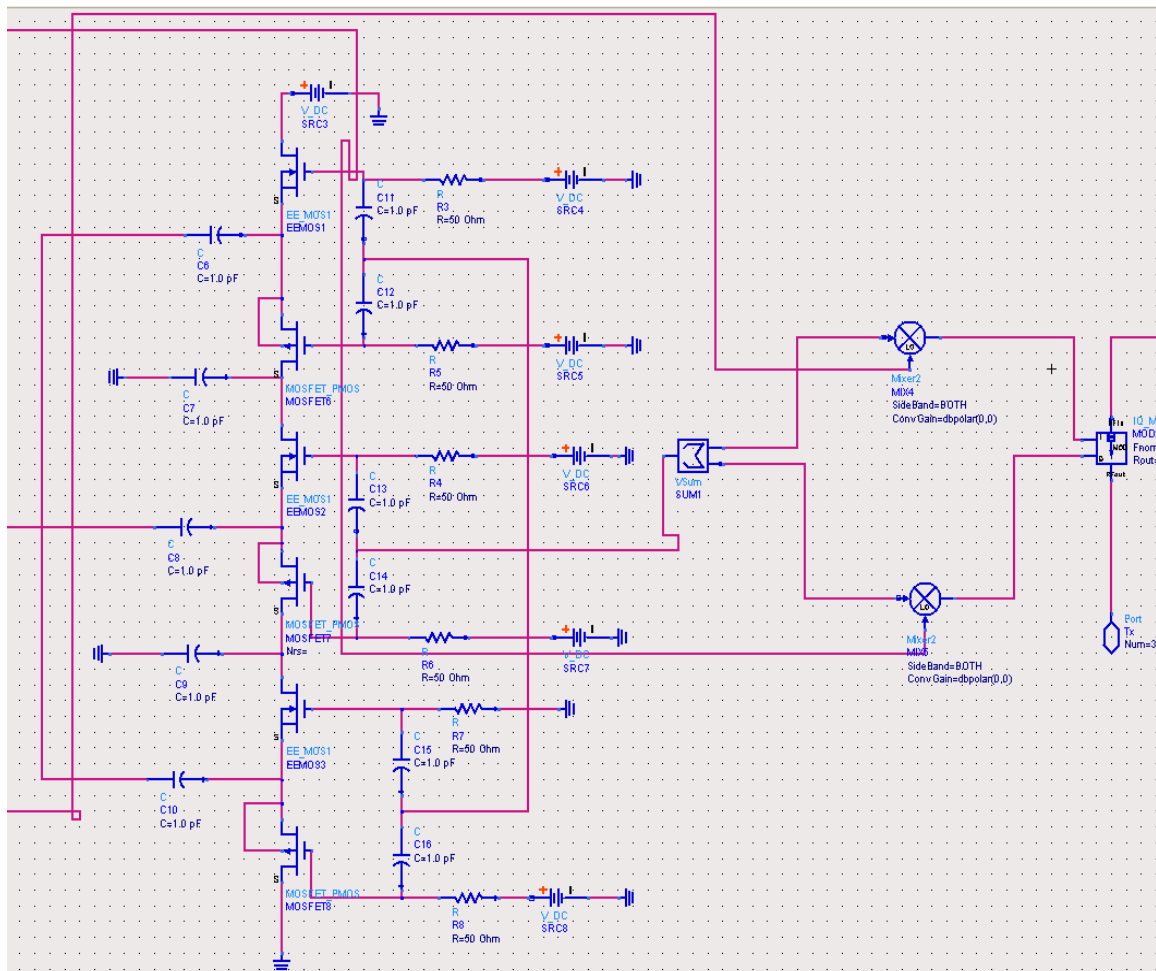


Figure: 5.3 Layout of power amplifier block circuit

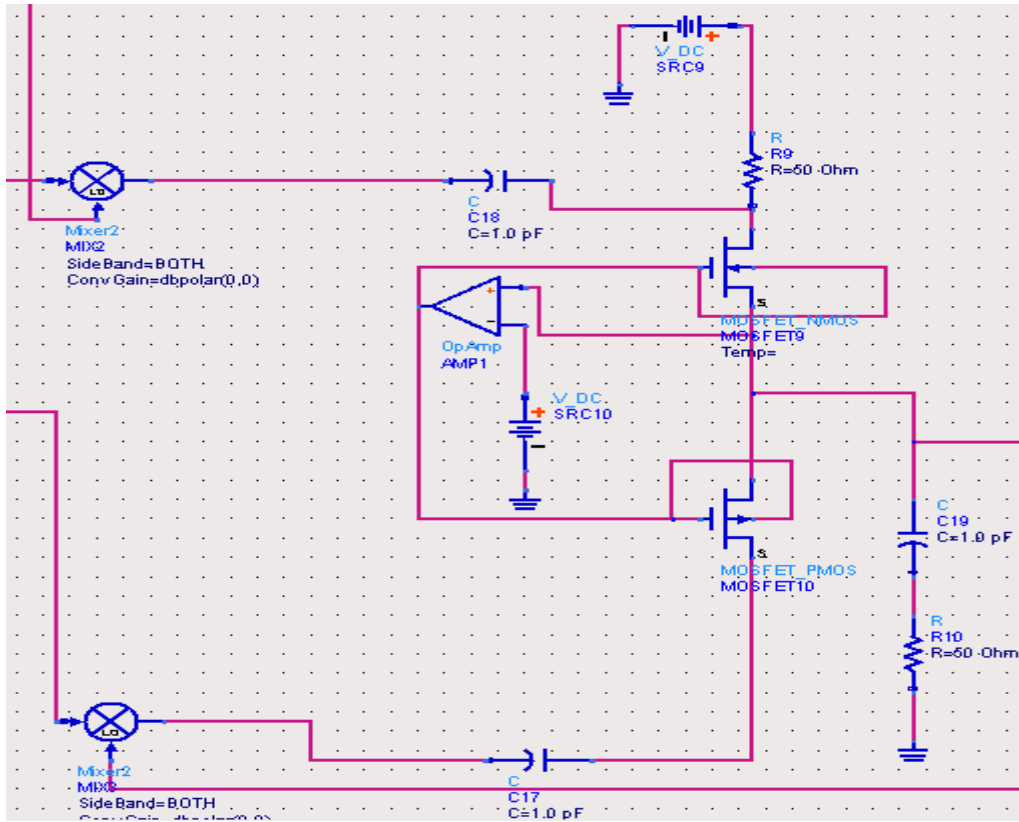


Figure: 5.4 Layout of Low noise amplifier block circuits

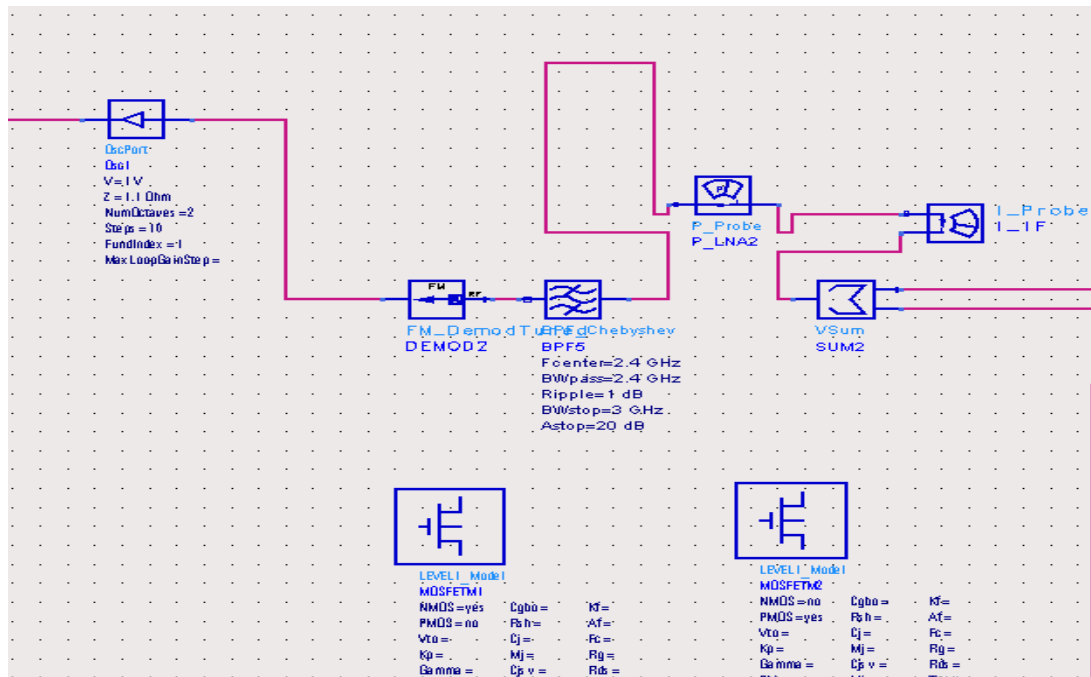


Figure: 5.5 Layout of IF block

RESULTS

Chapter 6

Results

6.1 Results and Measurements

According to the proposed solution, miniaturization, less operating voltage, energy utilization per unit time and simplicity are the performance parameters. The measurements and results are shown in following tables and figures. Table 1 shows the supply current and the supply voltage of each block of transceiver as shown below.

Table: 6.1 Transceiver blocks measurement

Transceiver blocks	Supply current (μA)	Supply voltage (v)
LNA/ mixer	293.55	≤ 1
Power Amplifier	347.948	≤ 1
Crystal Oscillator	595.5	1
Phase Locked Loop	645.0	1
IF	6667.4	1

In figure 6.1 image view of the RF transceiver circuit where all blocks connected to each other and the name of each block shown on the top of that circuit.

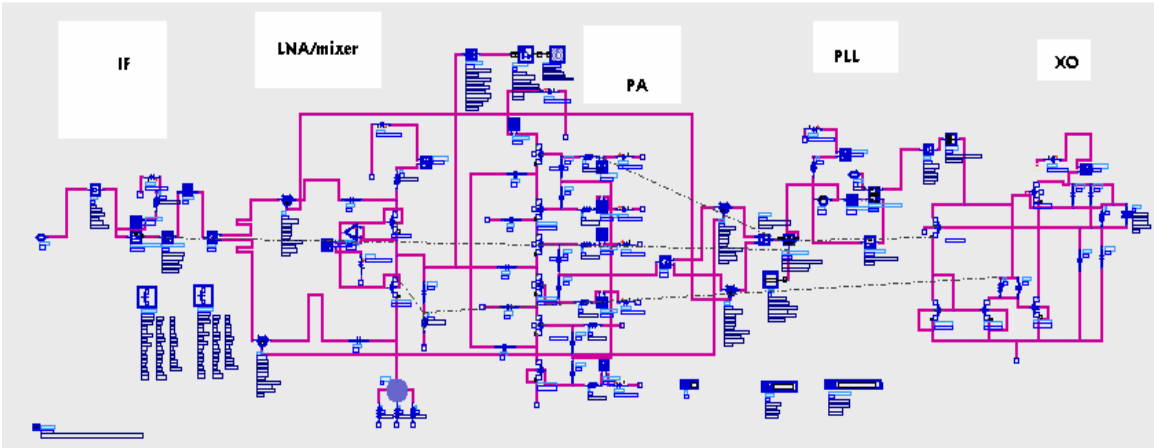


Figure: 6.1 RF Transceiver circuit including all five blocks together.

6.1.2 Budget Analysis

Budget analysis of some components which are very important and major on budget perspective of our transceiver are shown in figure 7.3 The graph shows four important components which play vital role in transceiver fabrication are summer, mixer, power supply, modulator/demodulator and Band pass filter and the quantity of these components are two, five, one, two and two respectively from bottom to top. Where the most expensive component is BPF (band pass filter) and summer is the cheapest, where MOD represents the modulator, MIX is mixer and PWR is the supply power.

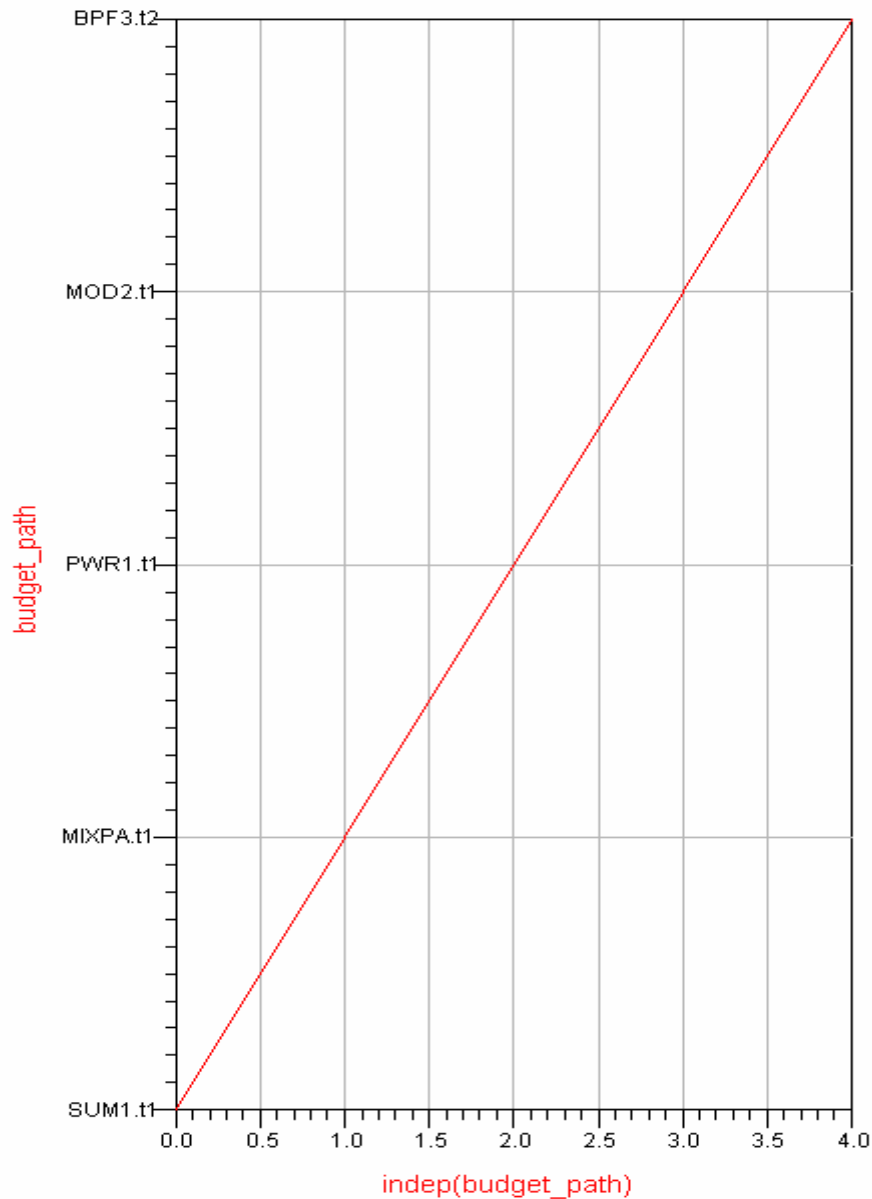


Figure: 6.3 Budget Analysis of some important components of transceiver.

6.2 Operating Frequency

In figure 6.4 the operating frequency starts from zero and after some time it increases its frequency to 2.4GHz and it stable at that point which is its operating frequency.

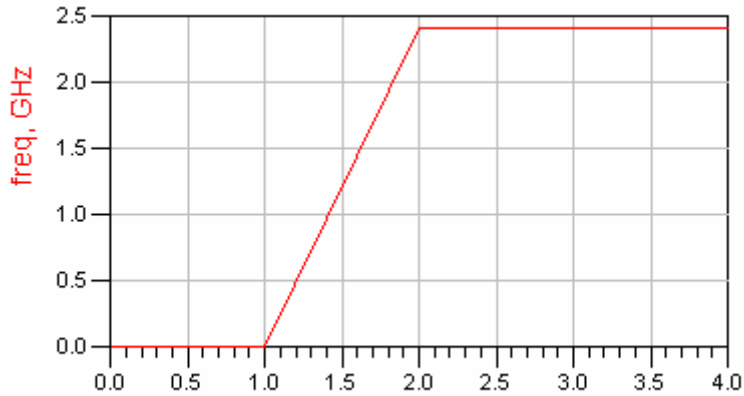


Figure: 6.4 Operating frequency

In figure 6.5 the graph between s parameter and frequency is shown the frequency starts oscillation from 2.4 GHz and stops on 3.4GHz.

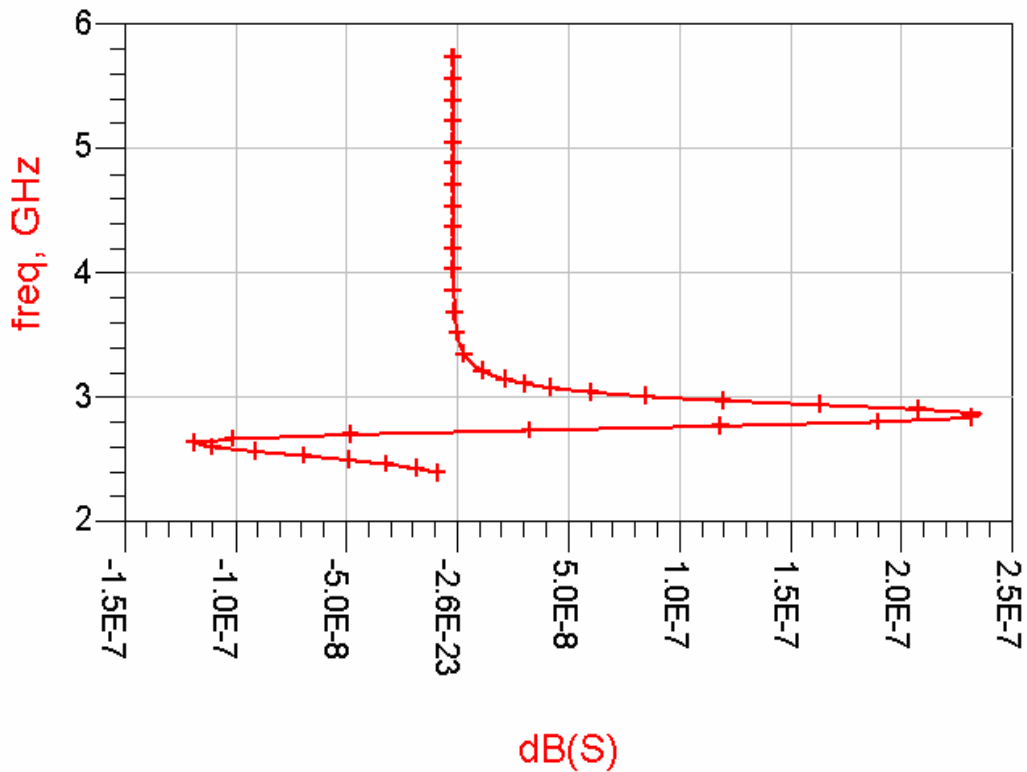


Figure: 6.5 Graph between S parameters and frequency in GHz.

In figure 6.6, a graph is shown between phase and frequency of PLL block which is the source of generating the operating frequency. The circles show the frequency in GHz. In x-axis frequency is shown where in y-axis phase is shown. It is clearly seen that phase at 90 gives the 2.4 GHz operating frequency.

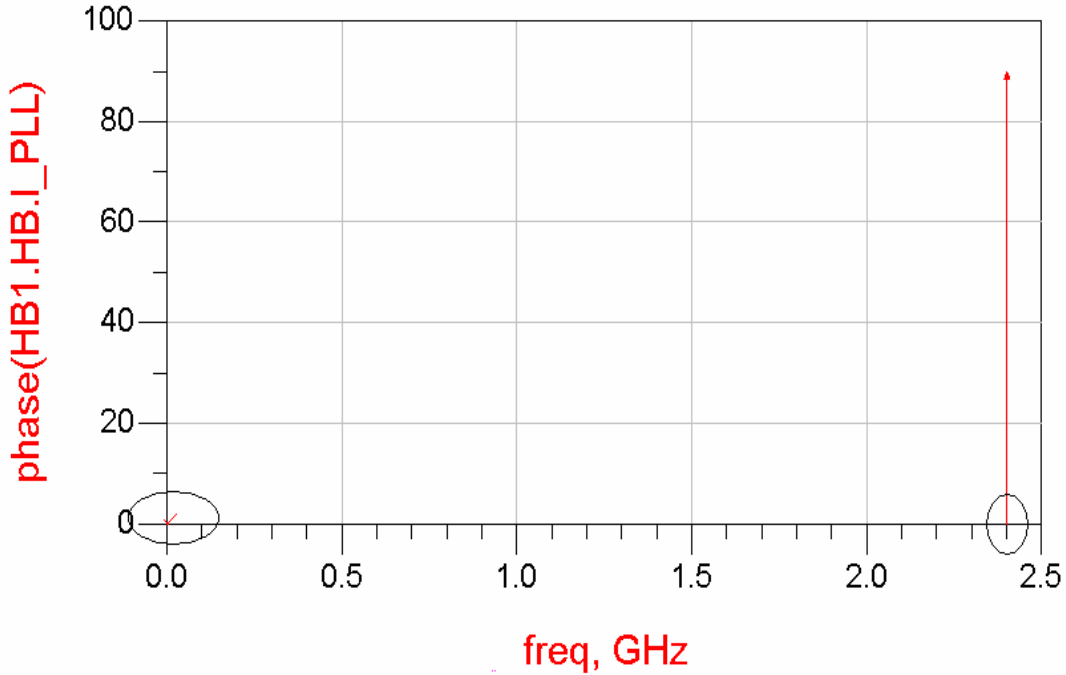


Figure: 6.6 PLL block operating frequency and phase relation.

Figure 6.7 shows the test of operating frequency in AC simulation of 0 to 100 nsec time.

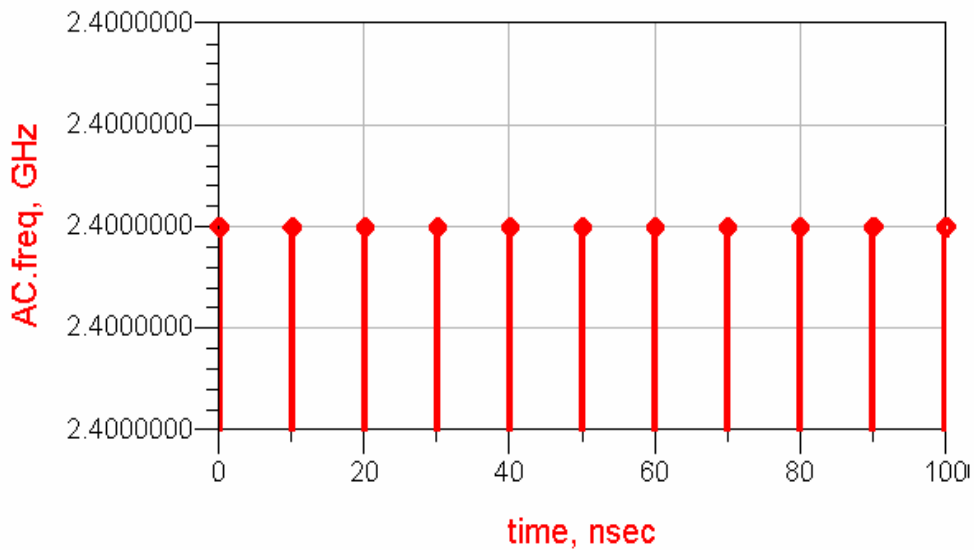


Figure: 6.7 Different Samples of Operating frequency between 0 to 100 nsec.

6.3 Comparison with reference researches

The table 6.3 shows the comparison between ULP2.4T and other reference transceivers. There are only four external components which are antenna, crystal, saw filter and battery. Components and their strength excluding PLL block which are used in the chip designing as follows.

- Modulator(1)
- Demodulator(1)
- Amplifier(1)
- Gill cell mixer(1)
- Band Pass Filter(1)
- Summer(2)
- Splitter(1)
- MOSFET(13)
- Capacitor(18)
- Resistor(14)

Table: 6.3 Comparison between ULP2.4T and previous work

Reference	Operating frequency	Operating voltage	Power consumption	Start up time	Modulation
B.P. Otis, 2004 [11]	1.9 GHz	1.2 volt	3mW in receiving mode	10 μ s	FSK
Alyosha Molnar, 2004 [5]	900MHz	3 volt	1.3mW in one mode	Not given	FSK
JJ Perez, 2006 [3]	2.4GHz	3.3 volt	5mW	Not given	QPSK
Chiung-An Che, 2007[2]	2.4GHz	1.8 volt	3.47mW for PA and 3.45mW for LNA	Not given	FSK
A.J. Davie, 2009 [1]	915MHz	1.5volt	1.6mW and 1.8mW	1200 μ s	FSK

ULP2.4T	2.4GHz	1 volt	133.8pW for LNA , 43.56pW for PA , 2.62mW for PLL and 2.92mW for XO	100ns	FSK
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6.4 Discussion

We proudly announce that ULP2.4T is low power, small size simple transceiver from wireless sensor networks. New 2.4GHz design is better as compare to reference researches described in table 6.3 specially from JJ Perez, 2006 [3] and Chiung-An Che, 2007[2] because they also use 2.4GHz operating frequency. Finally special comparison with Chiung-An Che, 2007[2] because FSK modulation and 2.4GHz frequency are the common points between ULP2.4T and [2], but in ULP2.4T all blocks are consumed very low power.

CONCLUSION AND FUTURE WORK

Chapter 7

Conclusions and Future work

7.1 Conclusions

In this thesis, we have proposed a simple and reliable idea to design simple circuit of an ultra low power small size RF transceiver. This proposed design also consumes less power and occupy less area. The transceiver contains five blocks which are power amplifier (PA), low noise amplifier (LNA), crystal oscillator (XO), Phase Locked Loop (PLL), and intermediate frequency(IF) and no inductor is used. Operating frequency is 2.4 GHz, operating voltage is 1 volt and fixed load is 50 ohms in our proposed RF transceiver. This intelligent design has reduced the overall size of this vital component of sensor node which ultimately results in lower power consumption and minimum cost. It is also intuited from the simulation results that number of components are also decreased by assigning the same job to other components in a distributed way. Moreover, the reduction of enable pins from five to three on the chip has automatically reduced the size of chip. Only four external components; crystal, SAW filter, antenna and battery are used.

7.2 Future Work

In future we need to design a low power small size transceiver for 4G or LTE, Wimax and all new coming technologies, because in future these technologies bring more advancement in their structure and need low power solution for their transmitting and receiving functionality. It means we need to design transceiver at 5.8GHz and higher frequency bands which are used for latest technologies.

We will design following transceivers in future

- Ultra low power 5.8GHz transceiver design for Wimax Applications.
- Ultra low power small size transceiver for Long term Evolution (LTE).
- Ultra Low power small size secure transceiver for Wireless security sensor Networks at ISM band.

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