Chapter 1

INTRODUCTION

1.1 An Overview of Ultra Wide Band

Ultra-wideband (UWB) technology is highly emerging with many features inviting major enhancements in today's wireless communications, Sensor networks, Wireless personal area networks radar and imaging systems. It can be used for future short-range indoor wireless communications.
UWB communications is involved in both research community and industry because of extremely wide transmission bandwidths, and having advantages including accurate position location and ranging, lack of significant fading, high multiple access capacity, extremely high data rates and easy material penetration [1]

UWB are mainly suited for short range communication systems like personal area networks and wireless sensor networks (WSN) because of the transmitted power restrictions. [2]

The UWB transmission is defined as any signal, which has a fractional bandwidth ($B_{fractional}$) greater than 0.20, or which covers a bandwidth greater than 500 MHz.

$$B_{fractional} \geq 0.2, \text{ 0r}$$

$$BW > 500 \text{ MHz}$$

The ratio of signal bandwidth to the center frequency in known as fractional bandwidth [3] and is given in equation 1.1:

$$B_{fractional} = \frac{BW}{f_{center}} = \frac{\left(f_{highest} - f_{lowest}\right)}{\frac{\left(f_{highest} + f_{lowest}\right)}{2}} \quad (1.1)$$

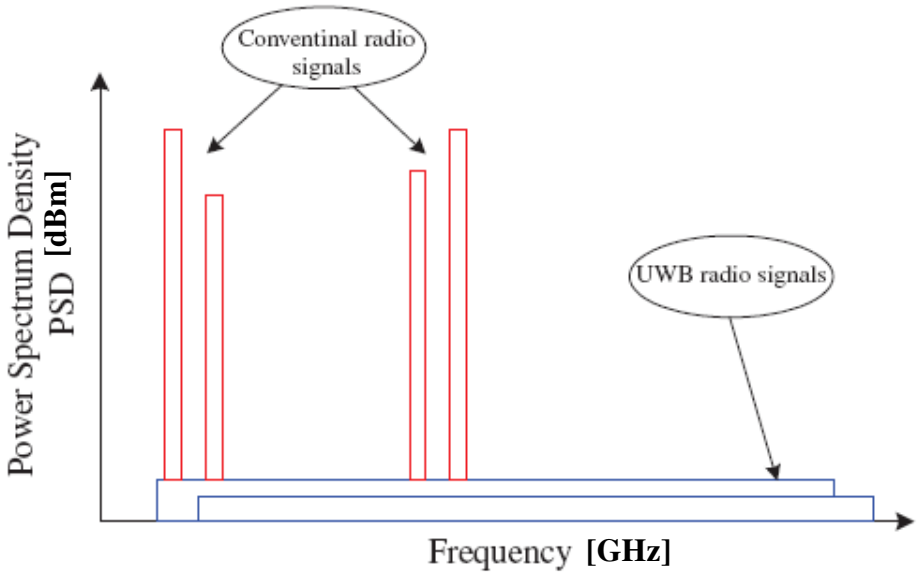

Figure 1.1: UWB radio signals versus conventional signals [3]

Where $f_{highest}$ is the high and f_{lowest} is the low transmitted frequencies at the –10 dB emission point, bandwidth is denoted as BW and center frequency as f_{centre}. Fig. 1.1 shows that fractional bandwidth of UWB is higher as compare to the conventional radio transmission. [3]

For the indoor and outdoor UWB systems the Federal Communications Commission (FCC) has assigned two masks. Figure 1.2 and Table 1.1 describes the indoor UWB communication system radiation limits which shows that the level of –41.3 dBm/MHz is in the frequency range of 3.1–10.6 GHz which is specified for protecting the existing radio services and to minimize the interference. [3]

Frequency Ranges	Indoor EIRP (dBm/MHz)	Outdoor EIRP (dBm/MHz)
960 MHz–1.61 GHz	–75.3	–75.3
1.61 GHz–1.99 GHz	–53.3	–63.3
1.99 GHz–3.1 GHz	–51.3	–61.3
3.1 GHz–10.6 GHz	–41.3	–41.3
Above 10.6 GHz	–51.3	–51.3

Table 1.1: UWB Radiation limits for indoor and outdoor communication

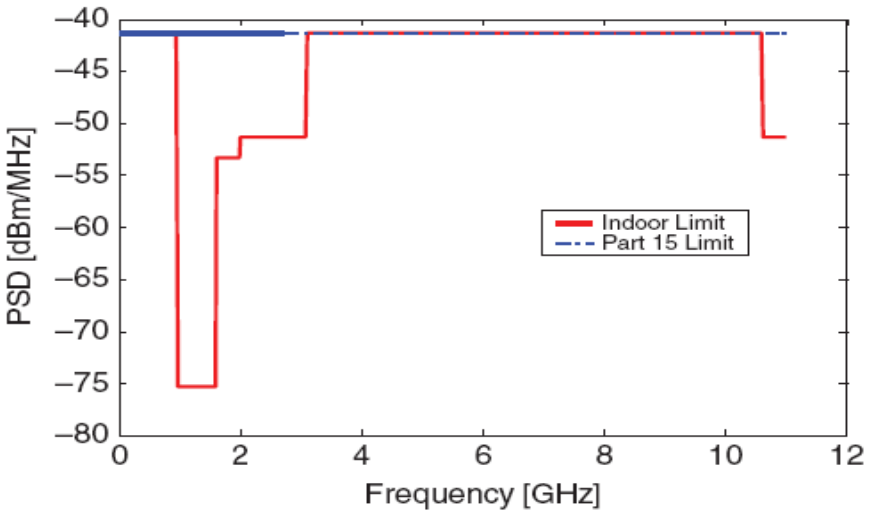

Figure 1.2: UWB Radiation limits of indoor communications [3]

For outdoor UWB communication systems the graph and values are shown in Figure 1.3 and Table 1.1 which shows that 1.6–3.1 GHz frequency range the outdoor radiation limit is 10 dB lower than the indoor mask. This shows that the outdoor UWB communications can handheld systems with no fixed infrastructure usage. [3]

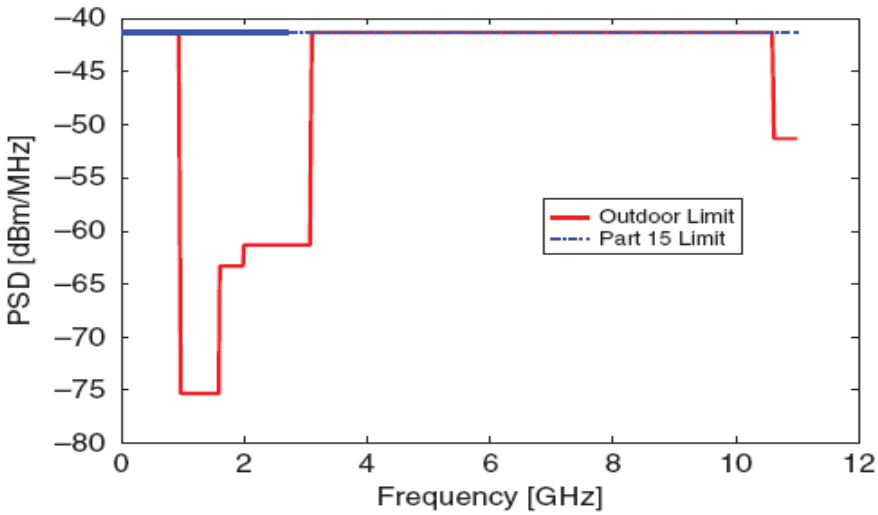

Figure 1.3: UWB Radiation limits of outdoor communications [3]

1.2 UWB Pulse:

The narrowband communications systems transmit and receive information with a specific carrier frequency for modulation. Figure 1.4 represents a narrowband signal in time domain and frequency domain but UWB communication is carrier less it uses picoseconds to nanoseconds pulses for transmission and reception which are very short in duration and having a very low duty cycle (less than 0.5 percent). [9]

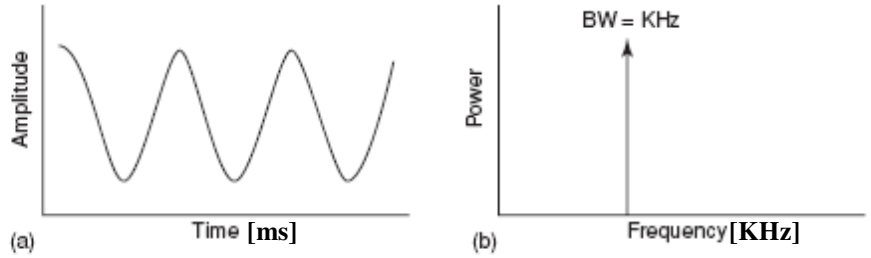

Figure 1.4 A narrowband signal in (a) time domain and (b) frequency domain [3]

1.2.1 Duty Cycle:

A simple definition for duty cycle is the ratio of the pulse presence time to the total transmission time as shown in equation 1.2:

$$\text{Duty Cycle} = \frac{T_{on}}{T_{on} + T_{off}} \quad (1.2)$$

Where T_{on} is the pulse presence time and T_{off} is pulse absence time. As UWB uses low duty cycle pulses with a very low average transmission in microwatts, which is a thousand times less than the transmission power of a mobile phone but the instantaneous power of a single UWB pulses can be relatively high because of very short duration transmission pulse. Due to which a longer battery life for handheld equipment can be achieved. Since frequency is inversely related to time, the UWB short duration pulses spread their energy from near DC to several gigahertzes (GHz) with very low power spectral density (PSD). Figure 1.5 shows UWB pulses in time and frequency domains. [9]

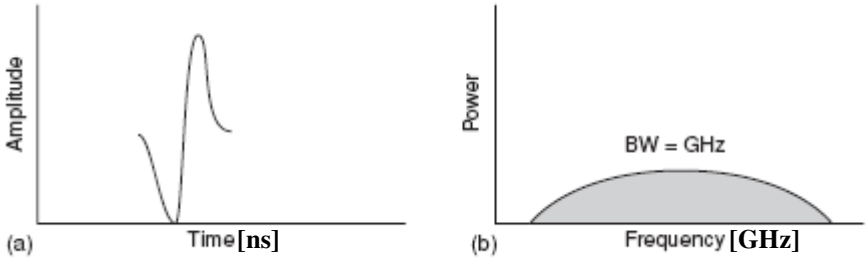

Figure 1.5 (a) The time domain UWB pulse and (b) The frequency domain UWB pulse [3]

1.3 Applications of UWB Communication

UWB technology is at its early stage so new applications are expected to include in next few years. The areas where UWB communication can be applicable for future development are as follow.

1.3.1 Wireless personal area networks:

WPANs are used for short range connectivity. The main services provided are distribution of very high quality and real time video/audio, file exchange, and it replaces cable for home entertainment systems. It also offers very high-rates at a short distance, the cost is low with a high power efficiency and low duty cycle so it is widely applicable to WPANs. [4]

1.3.2 Sensor networks:

A number of nodes are distributed across a wide area in sensor networks. There are static nodes e.g., tracking of mobile, if equipped on soldiers, firemen, or robots in military and emergency response situations. The requirements of sensor networks operation is that the cost and power should be low and multifunctionality options are embedded. UWB communication systems are used for gathering and transferring very high quantity of sensory data in a timely manner. The localization capability in UWB systems provides improved positioning accuracy in wireless sensor networks. [4]

1.3.3 Imaging systems:

The pulses of UWB radar are very short as compare to the dimensions of target. When the pulse is reflected off the target it changes the amplitude, time shift and also changes the shape of pulse. Because of this it provides sensitivity to scattering which is not provided in conventional radar signals. This property can be applicable to more applications that include ocean imaging, medical diagnostics and border surveillance devices [6], [7].

1.3.4 Vehicular radar systems:

As compare to motion sensors UWB based sensing can improve the resolution as it has high ranging accuracy with intelligent collision-avoidance. If UWB technology is introduced into vehicular entertainment as well as navigation systems then it is possible to download high data rate from airport off ramp, road-side, or gas station UWB transmitters. [4]

	Applications	
	Military and Government	**Commercial**
Data Communications	Secure LPI/D communications	Local and personal area networks
	Covert wireless sensor networks (battlefield operations)	Wireless streaming video distribution (home networking)
		Wireless sensor networks (health and habitat monitoring, home automation)
Radar	Through-wall imaging (for law enforcement, firefighters)	Medical imaging (remote heart monitoring)
	Ground-penetrating radar (for rescue operations)	Ground-penetrating radar (detection of electrical wiring, studs, etc. on construction sites)
	Surveillance and monitoring	Automotive industry (collision avoidance, roadside assistance)
		Home security (proximity detectors)
Localization	Personnel identification	Inventory tracking
	Lost children	Tagging and identification
	Prisoner tracking	Asset management

Table 1.2 Some UWB applications in military and commercial sectors

1.4 Challenges in UWB Communication:

There are many challenges involved in UWB communications [9].

1.4.1 Pulse-Shape Distortion:

Transmission characteristics of UWB pulses are different from those of continuous narrowband sinusoids. A narrowband signal has the property to be sinusoidal through the whole transmission. As compare to the weak and low-powered UWB pulses which can be distorted throughout the transmission link. Mathematically Friis transmission formula for the distortion is given in equation 1.3:

$$P_{rec} = P_{tran}\, G_{tran}\, G_{rec} \left(\frac{c}{4\Pi df} \right)^2 \quad (1.3)$$

Where P_{rec} is the power of received signal and P_{tran} is the power of transmitted signal, respectively; G_{tran} is the gain of transmitter antenna and G_{rec} is the gain of receiver antenna, d is the distance between the receiver and transmitted, f is the signal frequency and c is the speed of light. [9]

1.4.2 Channel Estimation:

The main issue for how to design a receiver in wireless communications systems is channel estimation. As it is not possible to measure every wireless channel among attenuations and delays of the propagation path so training sequences are used to estimate channel parameters. Due to wide bandwidth and reduced signal energy, UWB pulses undergo severe pulse distortion so it is needed that UWB receivers should correlate the received signal with a predefined template signal, and it is necessary to have the knowledge of the wireless channel parameters to predict the shape of the template signal which can match the received signal otherwise the channel estimation becomes very complicated. [10]

1.4.3 High-Frequency Synchronization:

Like any other wireless communications system the receiver and the transmitter should be synchronized in timely manner for UWB communication. Sampling and synchronizing of UWB pulses has a major limitation on the design of UWB systems so to sample these narrow pulses, very fast analog-to-digital converters (ADCs) are needed. [9].This requirement of fast ADCs is a big challenge for the development of UWB communication systems.

1.4.4 Multiple-Access Interference:

In communication systems many users transmit data independently over a transmission medium which is shared and is called as multiple-access communications system. These types of systems involve one or more than one receivers which should be able to separate users and detect information from the user of interest. Interference from other users with the user of interest is called multiple-access interference (MAI), which limits the channel capacity and the performance is also effected. The addition of MAI to the unavoidable channel noise and narrowband interference can significantly degrade the low-powered UWB pulses and make the detection process very difficult. As shown in Figure 1.6, represents a UWB multiple-access channel, separating each user's information from the combination of heavily distorted and low-powered UWB signals from all users is a very challenging task. [9]

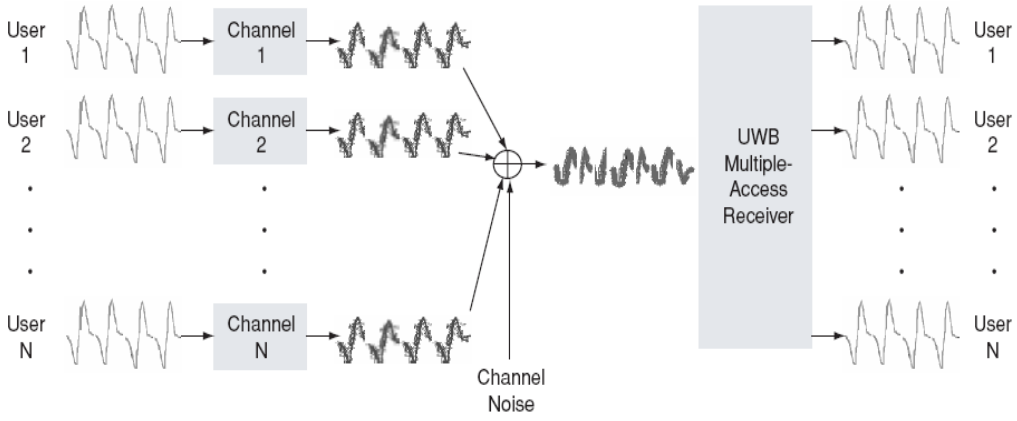

Figure 1.6 A UWB multiple-access channel [9]

Challenge	Problem
Pulse-shape distortion	Low performance using classical matched filter receivers.
Channel estimation	Difficulty predicting the template signals.
High-frequency synchronization	Very fast ADCs required.
Multiple-access interference	Detecting the desired user's information is more challenging than in narrowband communication.
Low transmission power	Information can travel only short distances.

Table 1.3 Challenges in UWB Systems

Chapter 02

UWB Channel Modeling

2.1 What is Channel:

Channel corresponds to the relationship between the transmitted and received signal [8]. The channel describes the design and performance of a system [11]. To characterize the channels properly precise channel models are needed, to mitigate all channel effects from the received signal so a reliable, realistic and accurate channel model is needed to enhance the system performance.

2.2 Types of Channels:

A lot of work has been done for traditional channel models but the results of that work cannot be directly applied to ultra-wideband. The major reason for this is the large bandwidth associated with UWB signal [8].

2.2.1 Narrowband Channel:

When the coherence bandwidth is greater than the bandwidth of the transmitted signal then the channel is said to be narrowband channel. The channel shows frequency non selective or flat fading [12]. All the received multipath components of a symbol arrives within a symbol time duration. The performance of the channel is not affected by the delay of individual multipath components [2]. These multipath components will interfere with one another at the receiver end. If the multipath components are large in number then the complex amplitude can be modeled as Rayleigh or Rician distribution [8] - [13].

2.2.2 Wideband Channel:

The channel is frequency selective as coherence bandwidth is less than the bandwidth of the transmitted symbol. The system performance is effected by the delay of multipath components. [13]. In order to remove the effect of these multipath components the delay axis is divided into bins where size of each bin is equal to the inverse of the bandwidth. It is assumed that each delay bin will contain multipath components.

2.2.3 Ultra-wideband Channel:

In ultra-wideband, the bandwidth is very large due to which the size of delay bins become small. A possibility is that there could be no multipath component falls in a delay bin.

2.3 UWB Channel Model:

UWB channel model which is free from fading and distortion is needed. The main limitation is that the power limitations for UWB communication decreases the coverage distance. For indoor communication because of low fading margin and power spectral density this type of system is preferred [14]. UWB indoor channel can be found in [15]. Two types of fading are involved in UWB communication named as small scale fading and large scale fading.

2.3.1 Small Scale Fading:

It is the fading which causes interference when number of versions of signal which is transmitter arrives at the receiver end at slightly different time [16]. This type of fading is mainly concerned with indoor communication as it is the fading with in $1m^2$ area. [8]. Saleh Valenzuela (S-V) model was selected for indoor UWB channel.

2.3.2 Large Scale Fading:

When the transmitted signal has impact of channel over large distance greater than 1m then it is known as large scale fading. The attenuation due to large objects that are in propagation path and distance are averaged which is the reason for large scale fading. The other term used for the large scale fading is known as path loss and is given in equation 2.1:

$$PL(d) = \overline{PL}(d_o) + 10n \log_{10}\left(\frac{d}{d_o}\right) + X_\sigma \qquad d \geq d_o \tag{2.1}$$

Where PL is the path loss, $PL(d_o)$ is the average path loss at distance d_o = 1m, n is the path loss exponent and X_σ is a Gaussian distributed random variable (in dB) with σ standard deviation also (in dB) [16].

2.4 Saleh Valenzuela Model:

The arrival of multipath components is in clusters [2], [1] and [17]. The number of multipath is a function of the measured bandwidth the environment [1] and is given in equation 2.2:

$$Nr = WT_d \tag{2.2}$$

Where *Nr* is the total number of multipath components, *W* is the signal bandwidth and T_d is the maximum delay.
In UWB the inter symbol interference also occurs which can be removed if the pulse of UWB are spaced closely in time [1]. This interference can be removed by using signal processing or equalization algorithms [1]. Two different categories of multipath are present: a cluster arrival and a ray arrival within a cluster. Four parameters are required to describe the model and modification of these parameters can be done according to required environment.

The parameters are as follow:

- Cluster arrival rate
- Ray arrival rate within a Cluster
- Cluster decay factor
- Ray decay factor within a Cluster

2.4.1 Cluster Arrival Rate:

By the building superstructure the clusters are formed [17]. Poisson process defines the cluster arrivals with mean cluster arrival rate given as Λ so the probability of getting *N* clusters in time *T* will be given in equation 2.3*:*

$$P\ (N\ Clusters\ in\ time\ T = N) = \frac{(\Lambda T)^N}{N!}\ exp\ (-\Lambda T) \qquad (2.3)$$

Where $T = T_1 + T_2 + \cdots + T_N$ and the arrival time of the *N*th cluster is denoted by T_N. The first cluster is always present. The exponential random variables describe the cluster interarrival time given in equation 2.4:

$$P\ (T_N \mid T_{N-1}) = \Lambda \exp\ [-\Lambda\ (T_N - T_{N-1})] \quad , \qquad N > 0 \qquad (2.4)$$

$1/\Lambda$ has the range of 10 to 50ns [1].

2.4.2 Ray Arrival Rate within a Cluster:

Rays are formed because of the objects within the vicinities of the transmitter and receiver [17]. It is donated by λ . A Poisson Process describes Ray arrival within a cluster making ray interarrival as exponential random variables given in equation 2.5:

$$P\left(T_{I,N} \mid T_{I-1,N}\right) = \lambda_N \exp\left[-\lambda_N \left(T_{I,N} - T_{I,N-1}\right)\right], \quad I > 0 \qquad (2.5)$$

Where $T_{I,N}$ is the arrival time of *I*th multipath in *N*th cluster and ¸*N* is the mean multipath arrival rate in the *N*th cluster. As we know that each cluster contains many multipath so the arrival rate is greater for the clusters which came later [1] and [24] by the combination of two Poisson processes given as [11] and [10] the ray arrival is modeled as in equation 2.6:

$$P\left(T_{I,N} \mid T_{I-1,N}\right) = \alpha \lambda_1 \exp\left[-\lambda_1 \left(T_{I,N} - T_{I,N-1}\right)\right] + (\alpha - 1)\, \lambda_2 \exp\left[-\lambda_2 \left(T_{I,N} - T_{I,N-1}\right)\right], \quad I > 0 \qquad (2.6)$$

Where α is the mixture probability while λ_1 and λ_2 are the ray arrival rates. One of the two arrival rate decays quickly which is shorter and contains strong multipath while the other is longer and contains slowly decaying paths [25].

2.4.3 Cluster Decay Factor:

The power decay profile describes the cluster decay factor [2]. It is denoted by Γ. The average power of the cluster is assumed to decay exponentially [25]. If the building walls were more reflective cluster decay factor, would increase [17]. Cluster decay factor is determined as the exponential decay of the peak power of the received cluster [13]. The first cluster arrival in each data set was normalized to amplitude of one and a time delay of zero and all other clusters arrivals in the same data sets are expressed relative to this time [26].

2.4.4 Ray Decay Factor within a Cluster:

There is an exponential decay in the average power of multipath within a cluster [14]. It is denoted by γ Multipath decay factor depends linearly on the arrival time of the cluster as shown in equation 2.7:

$$\gamma_N \alpha I_\gamma T_N + \gamma_O \qquad (2.7)$$

Where I_γ describes the increase of the decay constant with delay. The first ray arrival in each cluster was set to time zero and amplitude of one, and all other ray arrival within the clusters were adjusted accordingly [26].

The channel impulse response changes with time due to motion of the transmitter and receiver or due to change in channel itself in UWB. Such a channel is typically modeled using a tap-delay line approach [8].

Figure 2.1 shows the graph of Saleh-Valenzuela model [1].

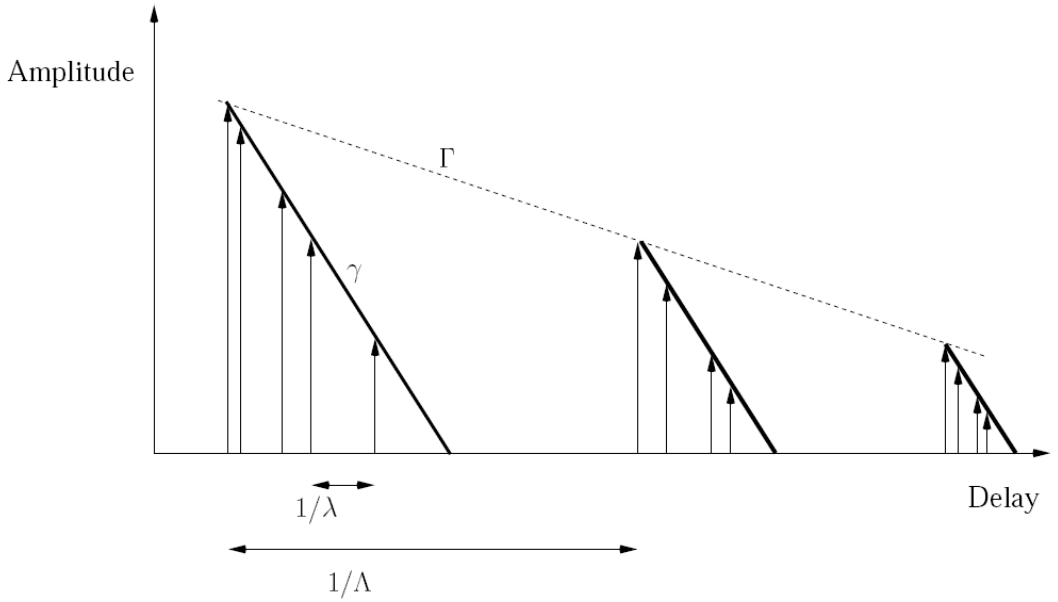

Figure 2.1 Saleh Valenzuela Model [1]

In S-V model the amplitude statistics is Rayleigh distributed [17]. But in UWB the measurement matched lognormal or Nakagami distributions [2]. Further the Nakagami distribution is preferred over lognormal distribution because:

1) Lognormal distribution can be approximated to Nakagami distribution for large values of the Nakagami-*m* parameter [2].

2) Even when the resolvable bin size is very small but still the Rayleigh distribution is valid for some environments [1]. Rayleigh fading was observed for industrial environment due to dense multipath scattering in [13]. This represents the observed phenomenon that late arriving paths are more numerous causing more fading [8]. For $m = 1$ Nakagami distribution is Rayleigh fading.

3) Nakagami-*m* distribution is a generalised distribution which often gives the best fit to landmobile and indoor-mobile multipath propagation environments, as well as to scintillate ionospheric radio links [27]. As can be seen that by just changing *m* in the Nakagami-*m* distribution different propagation scenarios can be achieved.

Chapter 03

Literature Survey

3.1 Background and Motivation:

ULTRAWIDEBAND communications systems have more than 500 MHz absolute bandwidth which is 20% of relative bandwidth. The spark-gap transmitter of Hertz and Marconi started UWB communication. In 2002, the frequency regulator in the United States allowed unlicensed UWB transmission, and other countries were expected to follow suit. It boosted the practical research on UWB communication systems. [11]

UWB is robust to fading having extremely high data rates, accurate positioning, multiple-access capabilities with low interference and a very low cost transceiver, making it the enabling platform for breakthrough applications in wireless communications. But there are a number of new technical challenges, most important is the new propagation models that describes and predict the traveling waves and its interaction with the surrounding environments, and after this prediction very efficient practical receiver architectures should be modeled. [32]

In frequency domain other signals potentially overlaps with UWB radio signals. So there is a possibility that other communication systems interfere regularly to cause interference which indicate the there should be maximum tolerable power to be present in the environment at any given frequency in UWB communication. [33]

For interference suppression there are two types of mechanisms in UWB communication one is time windowing over the duration of the short UWB pulse and second is the cross correlation at the receiver of the interference with the template which results in reduction of a narrowband interference due to the high correlation of the interference at times. [34]

When comes to channel prediction we seek to answer some questions the first one is that can we predict UWB channel, and if the prediction is possible then is it useful enough to remove the distortion effects observed. The study showed that how far the UWB channel can be predictable and with what accuracy which could help in making a very efficient UWB receiver architecture. [35]

The performance limits of a system can be modeled by the channel it is operating on. For system design and testing realistic channel models are needed. There is a fundamental difference between conventional propagation and UWB propagation, this impact is significant on system design. Many channel models have been proposed in the past [11]. Multipath component in

Ultra-Wide Band (UWB) systems produces channel impulse response so we have hundreds of transmitted symbols which require excessive memory requirement on equalizer implementation. In [18] a generic discrete-time z-domain transfer function estimation technique was proposed which states that an inverse system may be found for signal recovery.

In the entire wireless channels, the replicas (echoes) of the transmitted signal, is summed up from the reflecting, scattering, deflecting objects at the receiver. The major difference is that in a narrowband system the echoes received at the receiver is undistorted but attenuated, phase-shifted and delayed. But in UWB systems, the echoes received at the receiver suffers distortion of the transmitted pulses. Furthermore the shape of the arriving echoes varies from echo to echo. [31]

The UWB communications systems involves multipath fading which characterizes a number of multipath rays with propagation delays. The number of paths may range from very few to a multitude of paths. If we know the channel conditions then distortion effects at the receiver can be minimized, it is also possible for the transmitter to make an adjustment (pre-distortion). The proposed approach may be used as a means of aiding the detection of UWB pulses in the receiver and recovering the original signal from the distorted signal at the output of the transmission channel by designing an inverse system [19].

A novel technique for the estimation of UWB multipath channel distortion was introduced in [19]. It states that by designing an inverse system using the proposed formula for the channel it is possible to remove the effects of the multipath channel distortion on UWB pulses which increase the probability of detection at the receiver end.

The novel contribution of [18] is that this complete inverse system is indeed found and the corresponding recursive equation is provided for channel estimation.

Furthermore there is not enough literature on an efficient and detailed ASIC design flow for digital IC Design. Generic design flows are not suitable for the implementation. [20]

3.2 Limitation of Existing Relevant Literature:

The literature survey showed that the shape of Ultra-wide band signal is affected by multipath fading channel and it is not possible to identify different pulse shapes. So to tackle this problem a filter is needed this could equalize the effect of multipath fading.

The main limitation of existing literature was behavioral model HDL language for the equalizer. There was a vacuum between statistical channel modeling /equalizer for UWB and practical implementation of equalizer/ channel model.

In order to fulfill this gap between the two issues as above a mathematical model of memory efficient UWB equalizer is proposed and further more hardware implementation is done on Mentor Graphics IC Design tools.

3.3 Objectives:

After finding the desired difference equation for the inverse system, the main goal is to come up with efficient hardware architecture and its implementation. In order to achieve this arduous task first goal is to find an ideal architecture for memory efficient IIR filter. Secondly a realistic implementation of this architecture using advanced tools like mentor graphics.

In addition to this there is no efficient and detailed design flow for Mentor Graphics Digital IC Design tools. This work is going to propose a very efficient and detailed design flow for Mentor Graphics which could help in future implementations.

Chapter 04

Proposed Solution

4.1 Overview:

Channel with multipath fading is a main issue for UWB communications systems and is characterized by a number of multipath rays with propagation delays. The number of paths may range from very few to a multitude of paths. To tackle is issue channel conditions must be known and an inverse system must be designed which could cater the effect of multipath fading channel and distortion.

The proposed solution for the inverse system is Infinite Impulse Response (IIR) filter. IIR Filters works as signal conditioners. This accepts a signal at its input blocks the prespecified frequency components and allows the original at the output.

The main advantage of IIR filters is that it can generally approximate as a lower-order filter and it does not require extra memory for execution. IIR filters have a feedback element which makes them more suitable for efficient architecture of an inverse system design and because of this feedback they are also called as recursive filters.

As the Filters perform direct manipulations on the spectra of signals. The three main blocks which makes filter architecture are an adder, a multiplier, and a delay element.

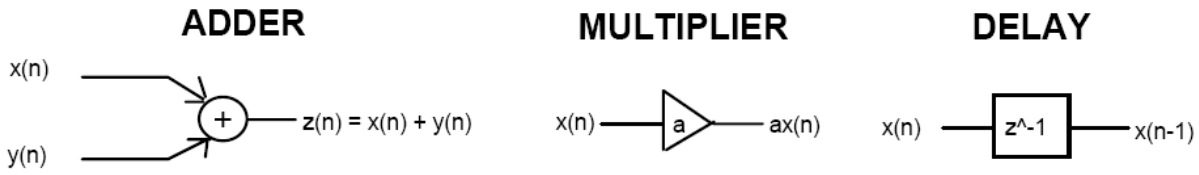

Figure 4.1: Building blocks of filter architecture.

To design a memory efficient IIR filter the conventional architecture shown in figure must be redesigned to an architecture which is memory efficient in nature by minimizing the delay elements.

4.2 Mathematical Modeling:

Mathematical modeling describes the desired difference equation for memory efficient IIR equalization filter.

4.2.1 Design Preliminaries:

The UWB CIR is constituted by aperiodically repeated clusters of negative-exponentially decaying segments, which gives a frequency having a gradually tapering magnitude. This specific characteristic of UWB CIR results in a memory-reduction for the receiver's IIR equalizer. A generic z-domain discrete-time transfer function derived for UWB CIR [11] with L tap-clusters, each tap having Nakagami-m distribution was given in [18] as described in equation 4.1.

$$H^{(L)}_{(UWB)}(z) = \sum_{m=0}^{\infty} \sqrt{\frac{E\xi_m}{T}} \xi_m \Phi(z) \left(1 - \frac{2}{T_d} \frac{1 - \sum_{l=1}^{L} \tau_l z^{-l}}{1 + \sum_{l=1}^{L} z^{-l}} \right) \quad (4.1)$$

where ξ_m is a statistically independent positive random variable having a Nakagami-m probability density function (PDF) with m=1 for rays within a cluster, $\Phi(z)$ is the z-transform of the UWB signaling-pulse of duration T and energy E, τ_l is the cluster arrival time expressed in nano-seconds and T_d is the sampling duration with Td $\gg \tau_l$. Introducing in equation (4.1) yields:

$$\Psi^{\dagger} = \sum_{m=0}^{\infty} \sqrt{\frac{E\xi_m}{T}} \xi_m \Phi(z) \quad (4.2)$$

$$H^{(L)}_{(UWB)}(z) = \Psi^{\dagger} - \frac{2\Psi^{\dagger}}{T_d} \left(\frac{1 - \tau_1 z^{-1} - \tau_2 z^{-2} \ldots - \tau_L z^{-L}}{1 + z^{-1} + z^{-2} \ldots + z^{-L}} \right) \quad (4.3)$$

Where $\Psi^{\dagger}$ is the Power Spectral Density (PSD) of the received UWB signal, which depends on both $\Phi(z)$ and on the tap-distribution determined by m. We can assume any particular signaling pulse shape and find the corresponding characteristics from [11]. Therefore, by employing any UWB signaling pulse shape having a linearly evolving phase-shift corresponds to equation (4.2), hence equation (4.3) can be approximated as:

$$H^{(L)}_{(UWB)}(z) \approx \frac{2\Psi^{\dagger}}{T_d} \left(\frac{1 - \tau_1 z^{-1} - \tau_2 z^{-2} \ldots - \tau_L z^{-L}}{1 + z^{-1} + z^{-2} \ldots + z^{-L}} \right) \quad (4.4)$$

As 1/Td is the sampling frequency, which is twice the bandwidth of the system and $\Psi^{\dagger}$ is the known PSD of the signaling-pulse, we introduce the product of these two constants as

$$\Psi^{\star} = \frac{2\Psi^{\dagger}}{T_d} \tag{4.5}$$

Finally, upon substituting equation (4.5) in equation (4.4), after a few algebraic simplifications we arrive at:

$$H^{(L)}_{(UWB)}(z) = \frac{Y(z)}{X(z)} = \begin{cases} \frac{\Psi^{\star} - \sum_{\zeta=1}^{L} \Psi^{\star}_{\zeta} z^{-\zeta}}{1 + \sum_{\zeta=1}^{L} z^{-\zeta}} \\ \Psi^{\star}_{\zeta} = \Psi^{\dagger} \tau_{\zeta} \qquad \text{for } \zeta = 1, 2, ..., L \end{cases} \tag{4.6}$$

This is the required transfer function of the UWB IIR equalizer.

4.2.2 Conventional IIR Equalizer Design:

This design hinges on the extension of equation (4.6) into a difference equation. Upon solving equation (4.6) for Y (z) we obtain:

$$H^{(L)}_{(UWB)}(z)\Big|^{(1)}_{IIR} : Y(z)\Big(1 + \sum_{\varphi=1}^{L} z^{-\varphi}\Big) = X(z)\Big(\Psi^{\star} - \sum_{\vartheta=1}^{L} \Psi^{\star}_{\vartheta} z^{-\vartheta}\Big) \tag{4.7}$$

Finally, taking the inverse z-transform of equation (4.7) gives the causal recursive difference equation for the conventional IIR UWB equalizer design in the form of:

$$y[n] = \Psi^{\star} x[n] - \sum_{\nu=1}^{L} y[n-\nu] - \sum_{\omega=1}^{L} \Psi^{\star}_{\omega} x[n-\omega] \tag{4.8}$$

The architecture modeling equation (4.8) is shown in Figure 4.2.

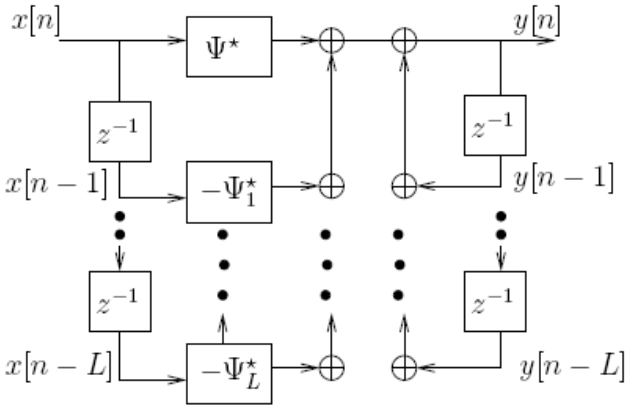

Figure 4.2 Conventional UWB equalizer

4.2.3 Memory Efficient IIR Equalizer Design:

The aim of this design is to combine the two delay-lines of Figure 4.2 into a single one, as equation (4.8) cannot be implemented by a single delay-line. But this design requires two recursive difference equations for interpreting the input-output relationship of the equalizer in order to rely on a single delay-line, which halves the IIR equalizer's memory requirement. These equations should be causal so that the new memory-efficient equalizer design remains practically realizable. To achieve this objective, we solve equation (4.6) again for Y (z), which yields:

$$H_{(UWB)}^{(L)}(z)\Big|_{IIR}^{(2)} : Y(z) : V(z)\left(\Psi^\star - \sum_{\Delta=1}^{L} \Psi_\Delta^\star z^{-\Delta}\right) \tag{4.9}$$

Where V (z) is given by:

$$V(z) = \frac{X(z)}{1 + \sum_{\Theta=1}^{L} z^{-\Theta}} \tag{4.10}$$

Finally, solving equation (4.10) for X (z) and taking the inverse z-transform of equations (4.9) and (4.10) we arrive at the required pair of causal recursive difference equations, which results in the halved-memory IIR UWB equalizer design as:

$$x[n] = \sum_{\alpha=0}^{L} v[n-\alpha] \tag{4.11}$$

$$y[n] = \Psi^\star v[n] - \sum_{\beta=1}^{L} \Psi_\beta^\star v[n-\beta] \tag{4.12}$$

The architecture modeling equations (4.11) and (4.12) is shown in Figure 4.3

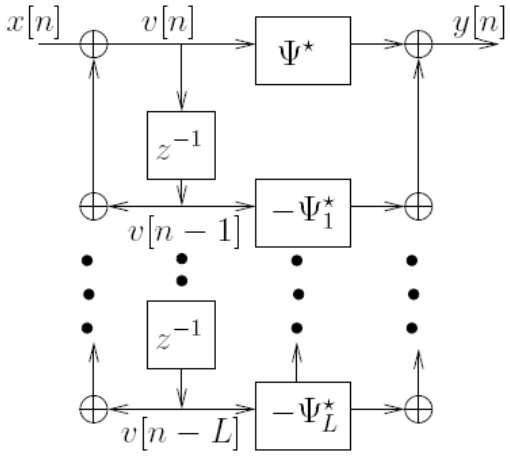

Figure 4.3 Memory Efficient UWB IIR equalizer

4.3 Improved ASIC Design Flow:

There are many stages involved in digital design flow which guides the design from the specification level to a verified GDSII layout. The starting point is block level specifications describing the requirement of the circuit. Many types of architectures may be examined keeping in mind the specifications when designing different digital blocks and implementing them, it is up to the requirement that you want to emphasis on the capacity of the architecture to achieve the required area, timing as well as power constraints. [22]

Digital ASIC Design flow can be partitioned into Front end design and Back end design.

4.3.1 Front end design:

Mentor Graphics Digital Design flow involves verification at each step of designing. The design flow is improved form [20] by introducing an extra level of verification at gate level which is also known as post synthesis verification .Figure 4.4 shows the front end design flow.

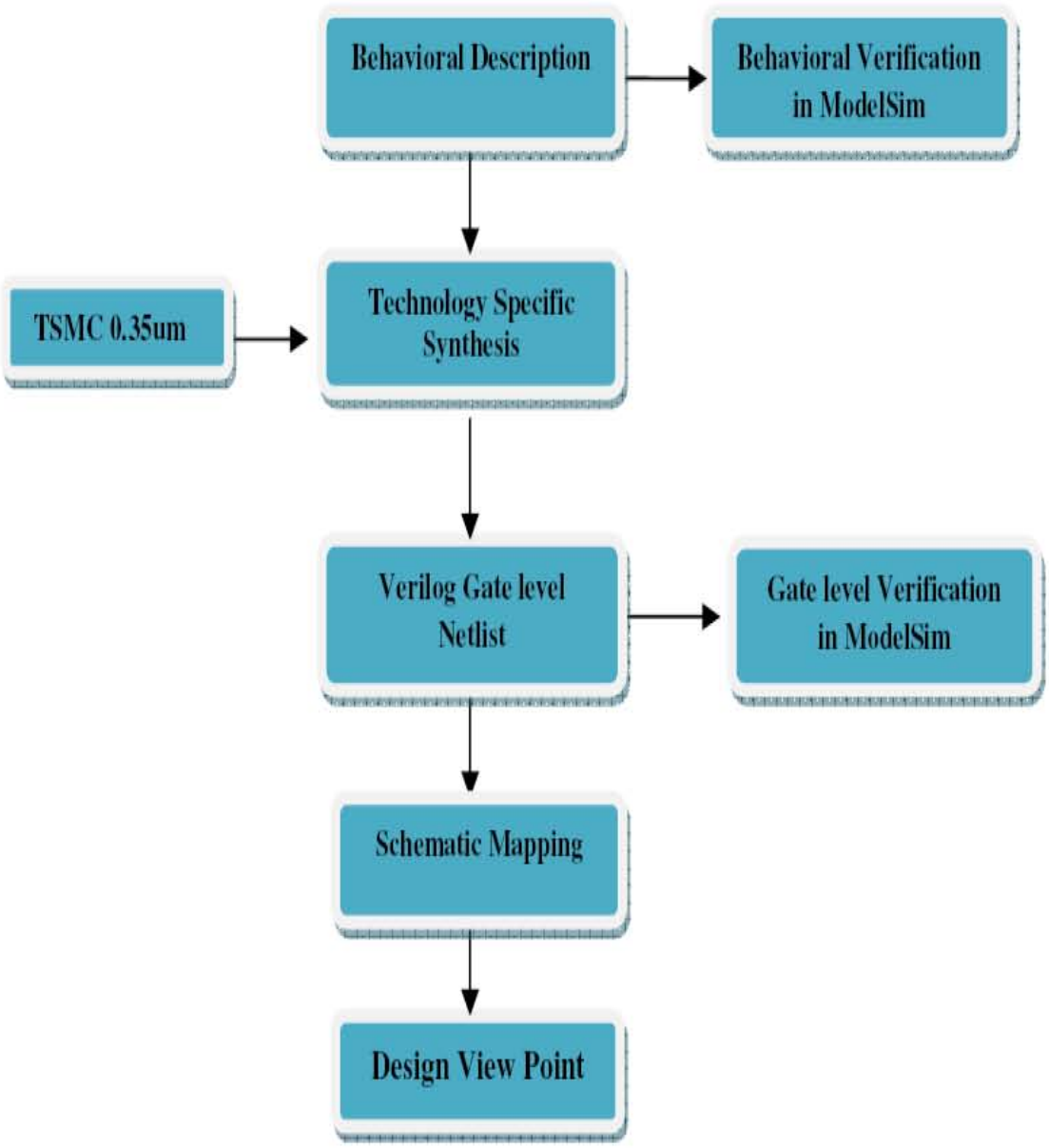

Figure 4.4: Front End Design Flow Chart

4.3.2 Backend Design

Figure 4.5 shows the backend design flow it describes the lowest level of abstraction possible in circuit description. In this stage, the circuit is described with respect to the silicon and other materials that go into the making of the IC.

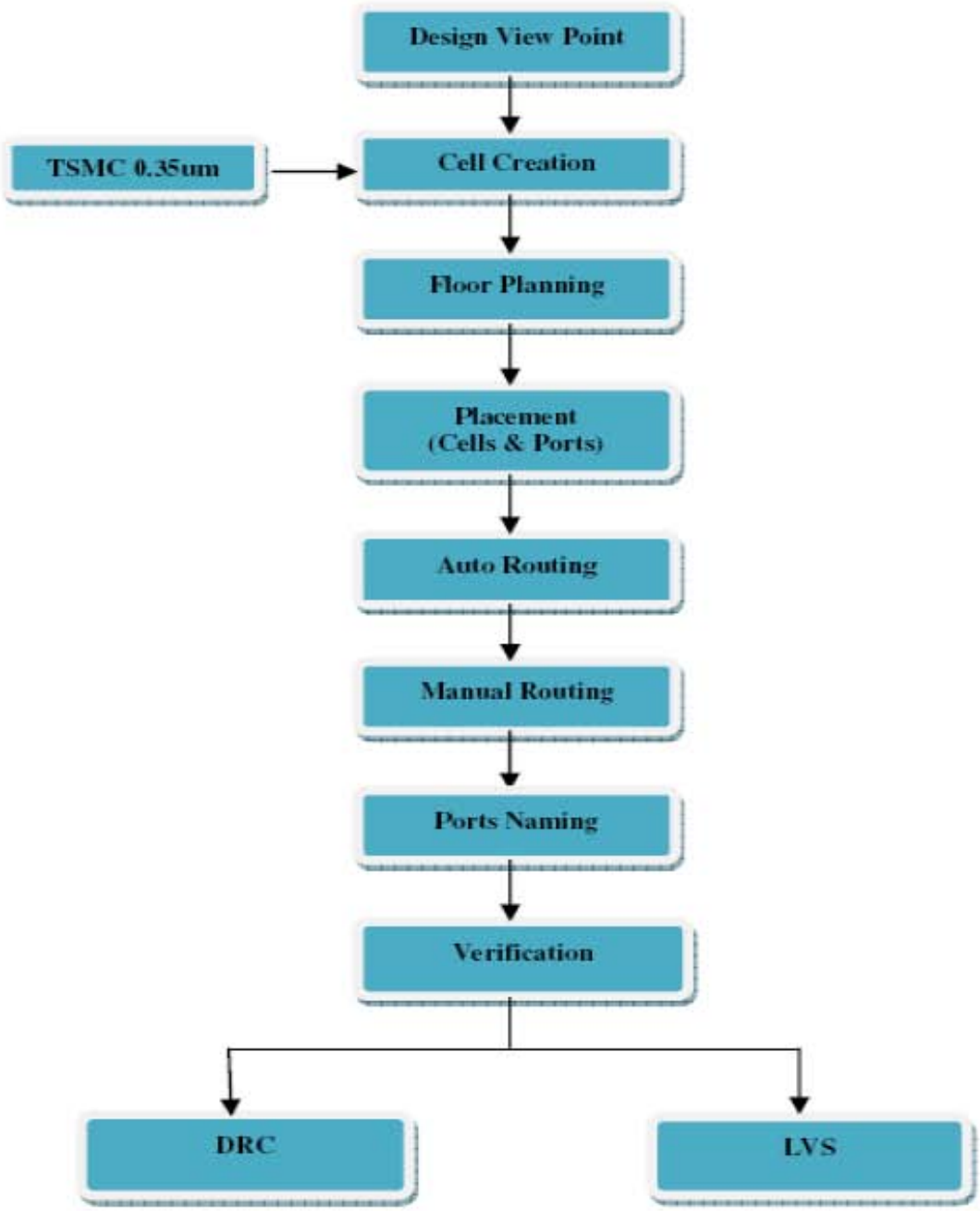

Figure 4.5: Back End design Flow Chart

4.3.3 Pads Placement Design Flow:

The input/ Output, VDD/GND Pads are used for connecting internal signals coming from the core cells of the integrated circuit to the external pins. Mainly I/O pads are organized into a rectangular Padframe. The smallest padframe available for the MOSIS chip fabrication "TinyChip" consists of 40 I/O pads, 10 on each side. TSMC0.35 TinyChip padframe is used for designing the complete IIR equalization filter chip for UWB.

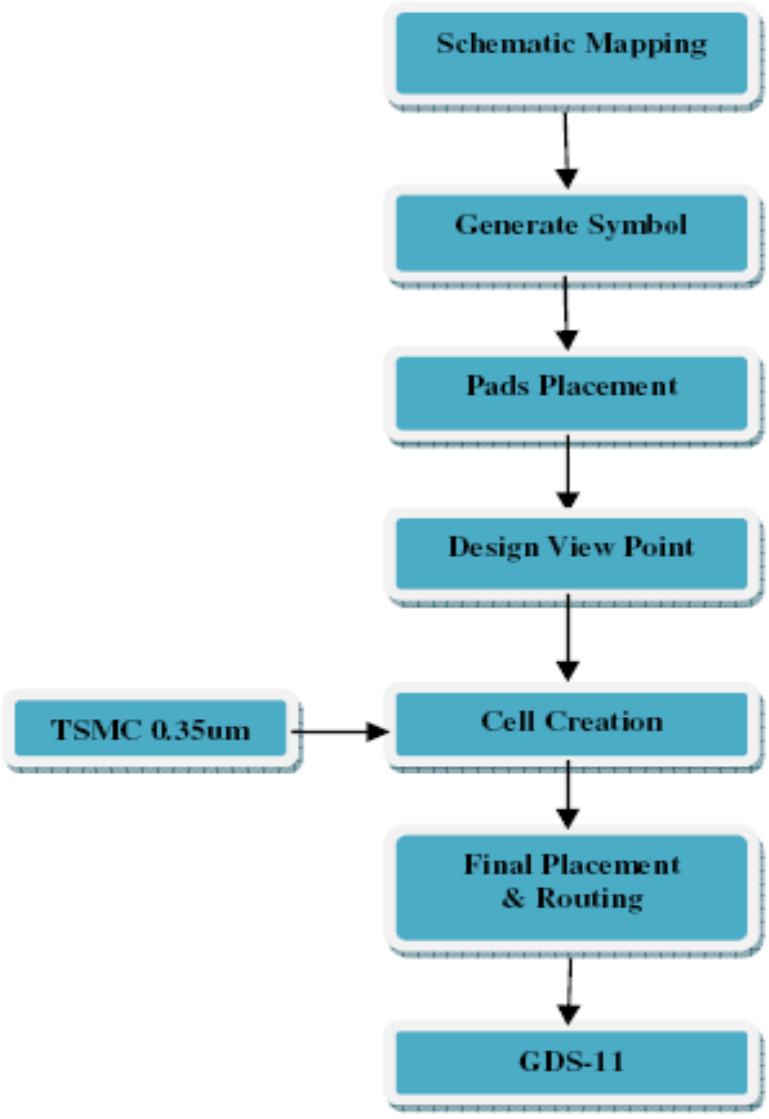

Figure 4.6: Pads Placement Design Flow Chart

Chapter 05

Implementation Results

5.1 BER Performance:

The distinct clusters of dense multipath components in UWB systems results in Channel Impulse Response (CIR) potentially spanning over hundreds of transmitted symbols, hence imposing excessive memory requirements on the equalizer's implementation. In [18] a generic discrete-time z-domain transfer function estimation technique was proposed, hypothesizing that a memory efficient Infinite Impulse Response (IIR) UWB equalizer implementation may be found. Hence this work showed that this memory efficient UWB IIR equalizer is indeed found and the corresponding design is implemented on ASIC. The proposed equalizer attains exactly the same BER performance as conventional equalizer, despite requiring only half the memory, as demonstrated against the benchmarker designs provided in [18], [19].

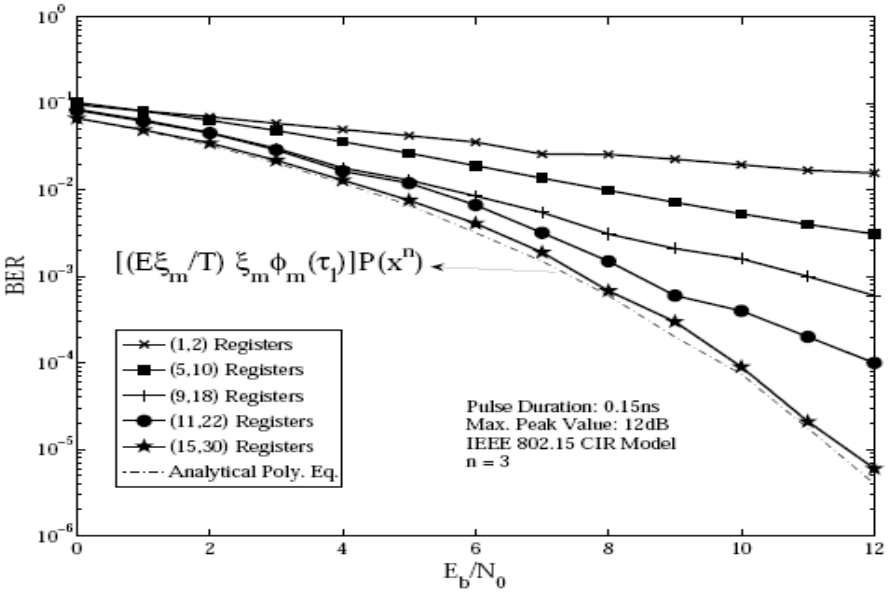

Figure 5.1: BER performance of the UWB equalizer designs

Figure 4.2 and 4.3, both of which are capable of approaching the analytical solution with a degree n = 3 in equation (19) of [19] and corresponding to (i, j) memory registers, where i is used in memory-efficient design and j is in the conventional design.

5.2 Design Methodology:

This work presents a very efficient design for Digital IC designing by implementing IIR Equalization filter which could be utilized as channel equalizer to cancel out distortion in UWB channel. The specialty of this filter design is the proposed memory efficient architecture which halves the memory requirement. Figure 5.2 shows the basic building blocks for the implementation

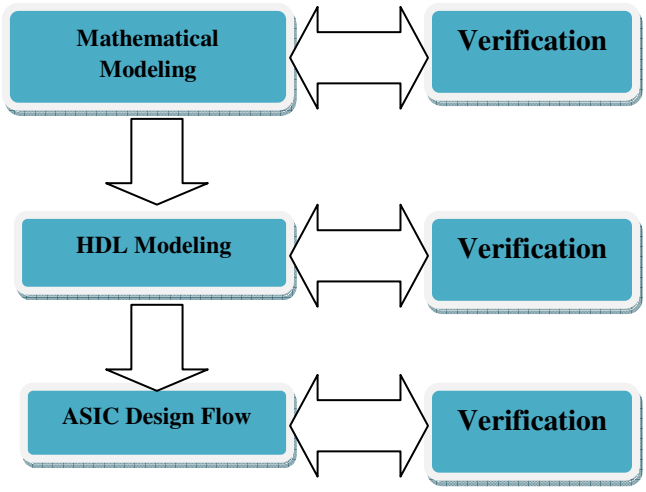

Figure 5.2 Basic Building blocks

.

5.3 HDL Modeling and verification:

The Mathematical model for memory efficient IIR Equalization filter is constructed in previous design step, it is necessary to come up with a circuit model to realize the design. For ASIC design, the behavior of systems is typically modeled in HDL using VHDL or Verilog for flexibility, portability and rapid prototyping [20] Fig. 5.3 shows the simulation results obtained from this behavioral VHDL model which was implemented on Mentor Graphic's ModelSim tool used for behavioral level verification.

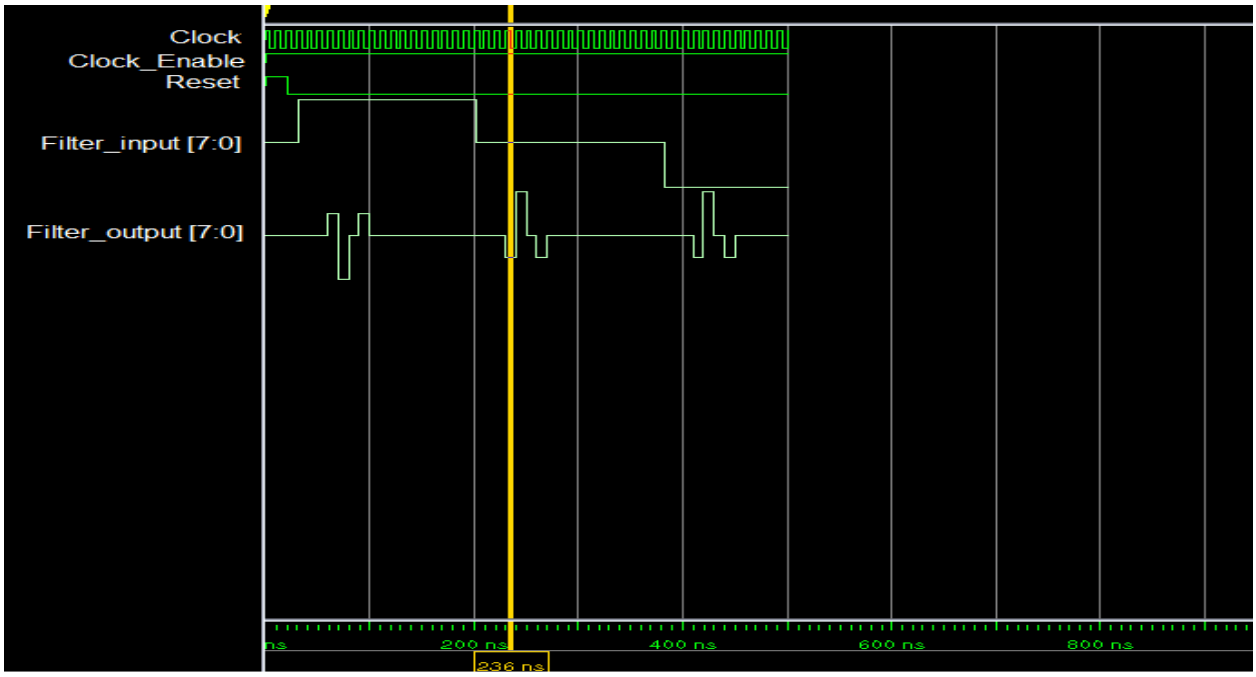

Figure 5.3 Behavioral Simulation result

5.4 ASIC Design Flow

Integrated circuits are much smaller both transistors and wires are shrunk to micrometer sizes, compared to the millimeter and centimeter scales of discrete components. Small size has the advantages of having smaller parasitic resistances, capacitances, and inductances which improves speed and power consumption. The high speed of circuit on chip is due to their small size smaller components [21]. ASIC uses Complementary Metal-Oxide Semiconductors (CMOS) technology which is the most common device used with large transistor count in today's integrated circuits. The CMOS are used because of their advantage of lower power requirements, high clock speed.

The Design Kit used for the implementation is ADK 3.1 which performs Standard Cell ASIC in which the designer uses predesigned logic gates the main advantage behind this is that the designers save time, money and reduce the risk by using a predesigned and pre-tested Standard Cell Library. Also each Standard Cell can be optimized individually. Digital ASIC Design flow can be partitioned into Front end design known as schematic design and Back end design known as physical design [23].

5.4.1 Front End Design:

This is the top level of abstraction which consists of different steps starting from the synthesis of behavioral VHDL description to technology specific gate level architecture and then the mapping

of this gate level architecture to transistor level Schematic. The technology used for the implementation is TSMC 0.35um.

5.4.1.1 Synthesis:

Synthesizing VHDL takes the design to next level of abstraction that is structural description. Synthesized netlist describes the constituent electronic components and necessary circuit details that combine to define a block of a system. The netlist includes primitives like logic gates and large pre designed blocks called standard cells. Extensive simulations are performed to verify the desired operation. Successful simulations ensure building of an electronic circuit to match the behavioral description. Clock Frequency is any important factor to be taken care of for High-performance digital integrated circuit which Gauge the ability of a circuit to work at the specified speed, and it can be used to measure delay at numerous steps. Clock frequency specifies the clock periods for all clocks in the design. Clock frequency used for the implementation of IIR Equalizer is 50MHz and the design is optimized to cater for delays. Leonardo Spectrum a Mentor Graphics Synthesizer tool is used for this process.

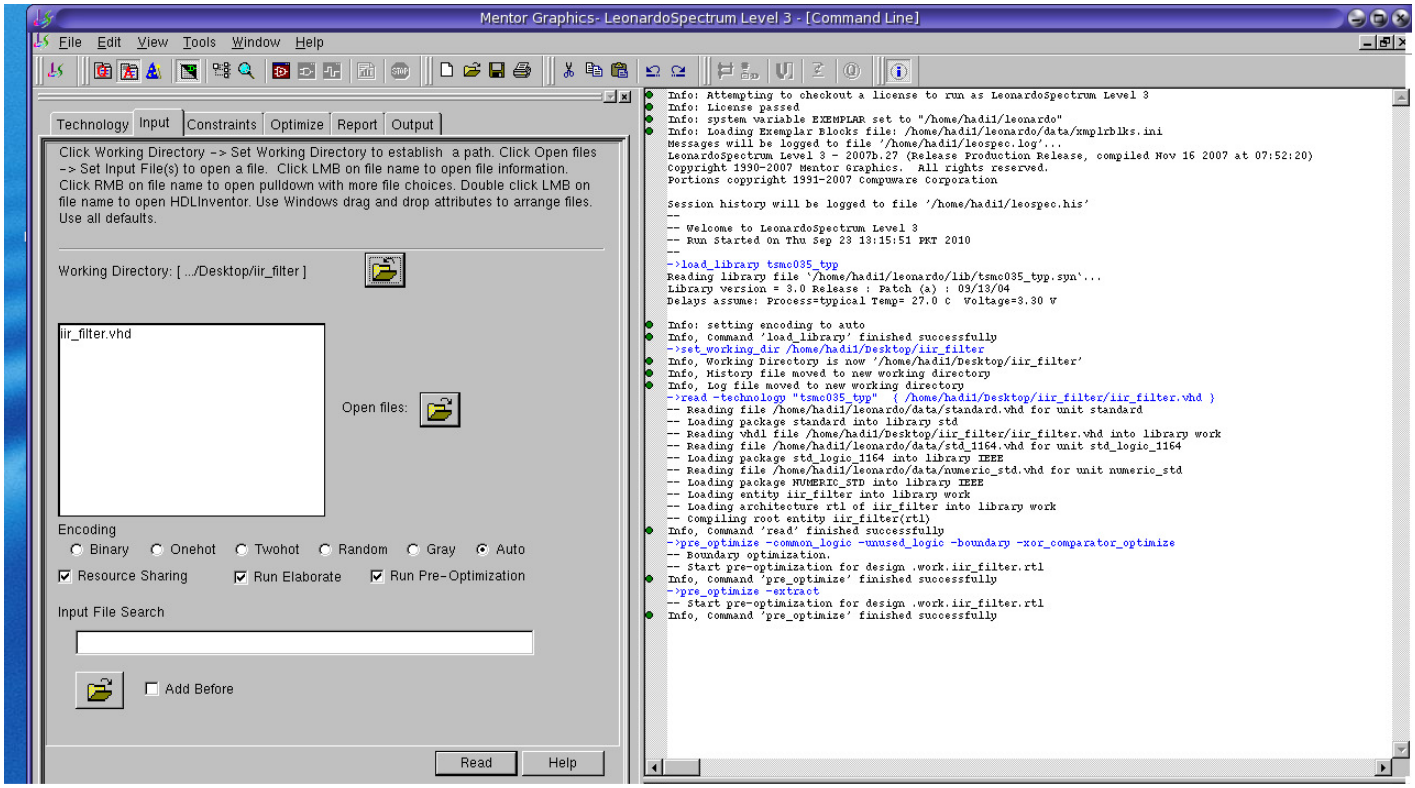

Figure 5.4 Leonardo Spectrum Front environment for VHDL input

The top block showing all the inputs and outputs in described in figure 5.5

Figure 5.5 Top Block of Memory efficient IIR Equalization Filter

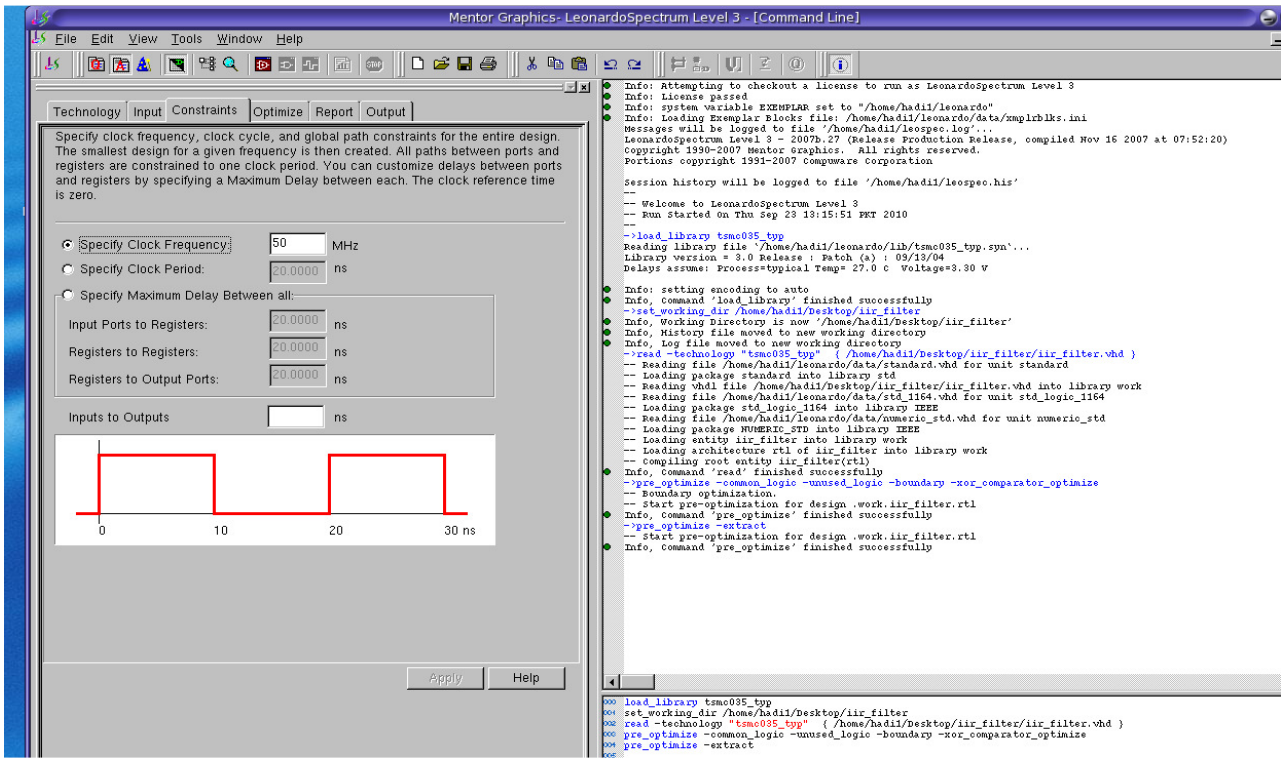

Figure 5.6: Clock Frequency Specification

5.4.1.2 Critical path:

The path which provides the maximum delay between inputs and outputs is known as critical path. A trace back method is used to find the circuit's critical path. Figure 5.7 shows the critical path of IIR Filter design [30]. The calculation of data arrival time and data required time is needed.

The time utilized by a signal to arrive at a certain point is known as data arrival time. For a clock signal the time 0.0, is often taken as the arrival time. A knowledge of delay time for all the components in needed for the calculation of data arrival time [30].

The data required time is the latest time at which a signal can arrive without making the clock cycle longer than desired [30].

The slack is the difference between the data required time and data the arrival time. A positive slack implies that the data arrival time can be increased without affecting the overall delay of the circuit and negative slack implies that there is a path delay which should be removed.[30]

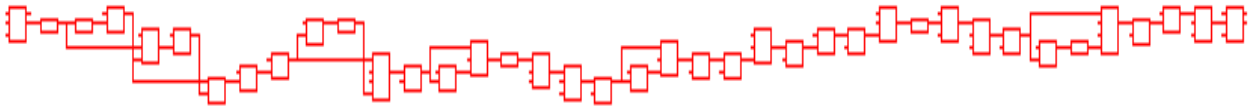

Figure 5.7: Critical Path for IIR Filter Design

Critical Path Report

Critical path #1, (path slack = 6.7):

Critical path #1, (path slack = 6.7):

NAME	GATE		ARRIVAL	LOAD
clock information not specified				
delay thru clock network			0.00 (ideal)	
reg_delay_section1(0)(0)/QB	dffr	0.00	0.48 up	0.01
ix4679/Y	inv02	0.18	0.65 dn	0.07
ix4753/Y	inv02	0.27	0.92 up	0.08
ix3588/Y	or02	0.38	1.30 up	0.04
ix3586/Y	oai21	0.31	1.62 dn	0.06
ix453/Y	xor2	0.62	2.24 up	0.03
ix3616/Y	xnor2	0.32	2.56 dn	0.07
ix495/Y	xor2	0.68	3.24 up	0.03
ix497/Y	xnor2	0.22	3.46 dn	0.03
ix3625/Y	xor2	0.64	4.10 up	0.03
ix499/Y	inv01	0.10	4.20 dn	0.01
ix3635/Y	aoi22	0.34	4.55 up	0.04
ix3633/Y	xnor2	0.32	4.87 dn	0.04
ix571/Y	xnor2	0.30	5.17 up	0.04
ix3670/Y	mux21_ni	0.47	5.64 dn	0.03
ix585/Y	inv01	0.16	5.81 up	0.01
ix645/Y	mux21_ni	0.38	6.18 up	0.04
ix1027/Y	mux21_ni	0.40	6.58 up	0.04
ix1073/Y	xnor2	0.28	6.86 dn	0.04
ix1075/Y	xnor2	0.29	7.15 up	0.04
ix3882/Y	mux21_ni	0.47	7.62 dn	0.03
ix3880/Y	xnor2	0.21	7.83 up	0.02
ix1171/Y	xnor2	0.29	8.12 dn	0.04
ix1405/Y	mux21_ni	0.47	8.60 up	0.02
ix1453/Y	xnor2	0.23	8.82 dn	0.03
ix3492/Y	xnor2	0.42	9.24 up	0.09
ix4136/Y	xnor2	0.34	9.58 dn	0.04
ix4150/Y	mux21_ni	0.52	10.10 up	0.03
ix1907/Y	inv01	0.10	10.20 dn	0.01
ix1953/Y	mux21_ni	0.38	10.58 dn	0.04
ix4179/Y	aoi21	0.35	10.93 up	0.02
ix1989/Y	xnor2	0.29	11.23 dn	0.03
ix4176/Y	xor2	0.64	11.87 up	0.03
ix1991/Y	inv01	0.10	11.97 dn	0.01
ix4182/Y	aoi22	0.27	12.24 up	0.02
ix2013/Y	xnor2	0.27	12.51 dn	0.03
ix3401/Y	xnor2	0.18	12.69 up	0.01
ix2874/Y	mux21	0.18	12.88 dn	0.02
reg_sos_pipeline1(7)/D	dffr	0.00	12.88 dn	0.00
data arrival time			12.88	

data required time (default specified - setup time)	19.53
data required time	19.53
data arrival time	12.88
slack	6.65

Figure 5.8 Critical Path Report

Figure 5.8 show the Critical path report which describes that the data required time was 19.53 and the data arrival time is 12.88 so the slack is 6.65.The successfully synthesis process results in an output gate level netlist.

5.4.1.3 Design Information Report:

The design information report shows the number of gates, number of ports and accumulated instances used for the design of memory efficient IIR filter

```
Number of ports :                          19
Number of nets :                         1021
Number of instances :                     991
Number of references to this view :         0


Total accumulated area :

Number of gates :                        1673

Number of accumulated instances :         991
```

5.4.1.4 Post Synthesis Verification:

Verification of gate level netlist is performed by simulating it using ModelSim. The results at this stage are matched with the previous results being observed at behavioral level. This verification is termed as post-synthesis verification as shown in Figure 5.9. After verification the schematic mapping is being performed.

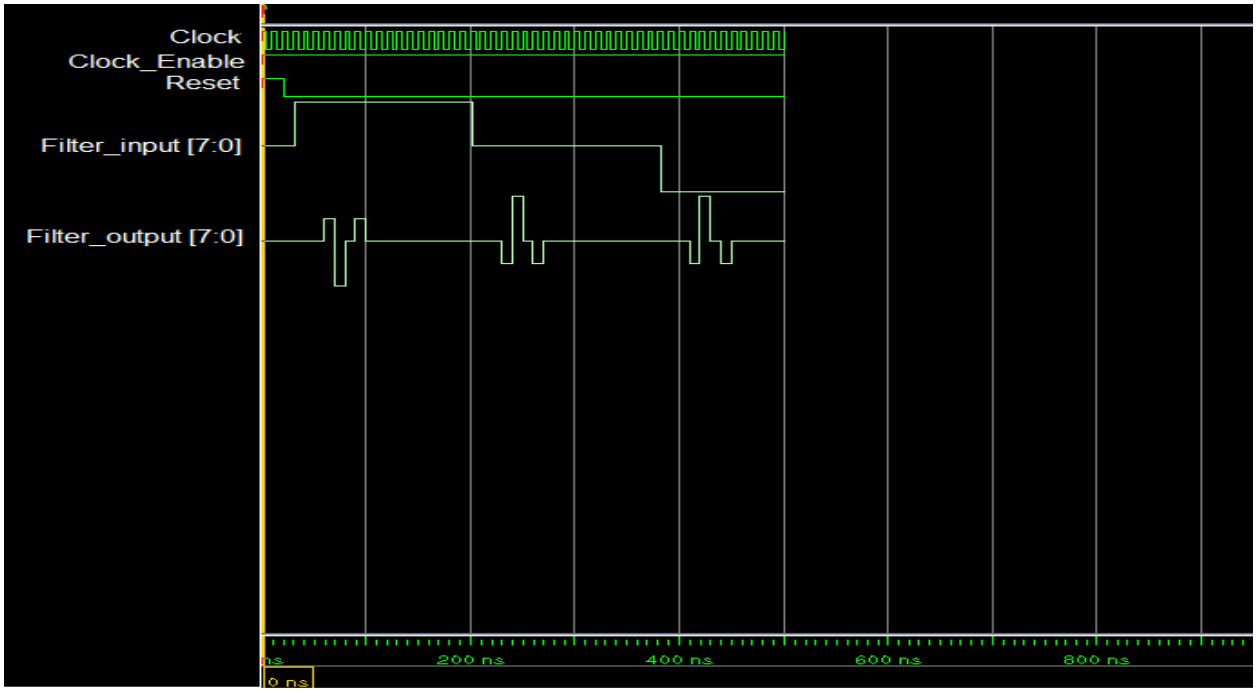

Figure 5.9 Post Synthesis verification

5.4.1.5 Schematic mapping:

Schematics mapping can be considered to be at a lower level of abstraction since the synthesized gate level design is mapped to transistor level schematic. Just as in the previous stage, various electronic components like logic gates and standard cells are placed and interconnected to make the circuit blocks. Now the functionality of these logic gates and standard cells are controlled by MOS transistors. Figure 5.10 show the gate level schematic Sheet#1 of IIR Filter design which is driven by MOS transistor. The primary goal of schematic mapping is to create schematic driven layout (SDL) viewpoints, to be used for backend designing. Mentor Graphics Design Architect tool is used for this purpose. The overall behavior of equalization filter is described in Table. 5.1

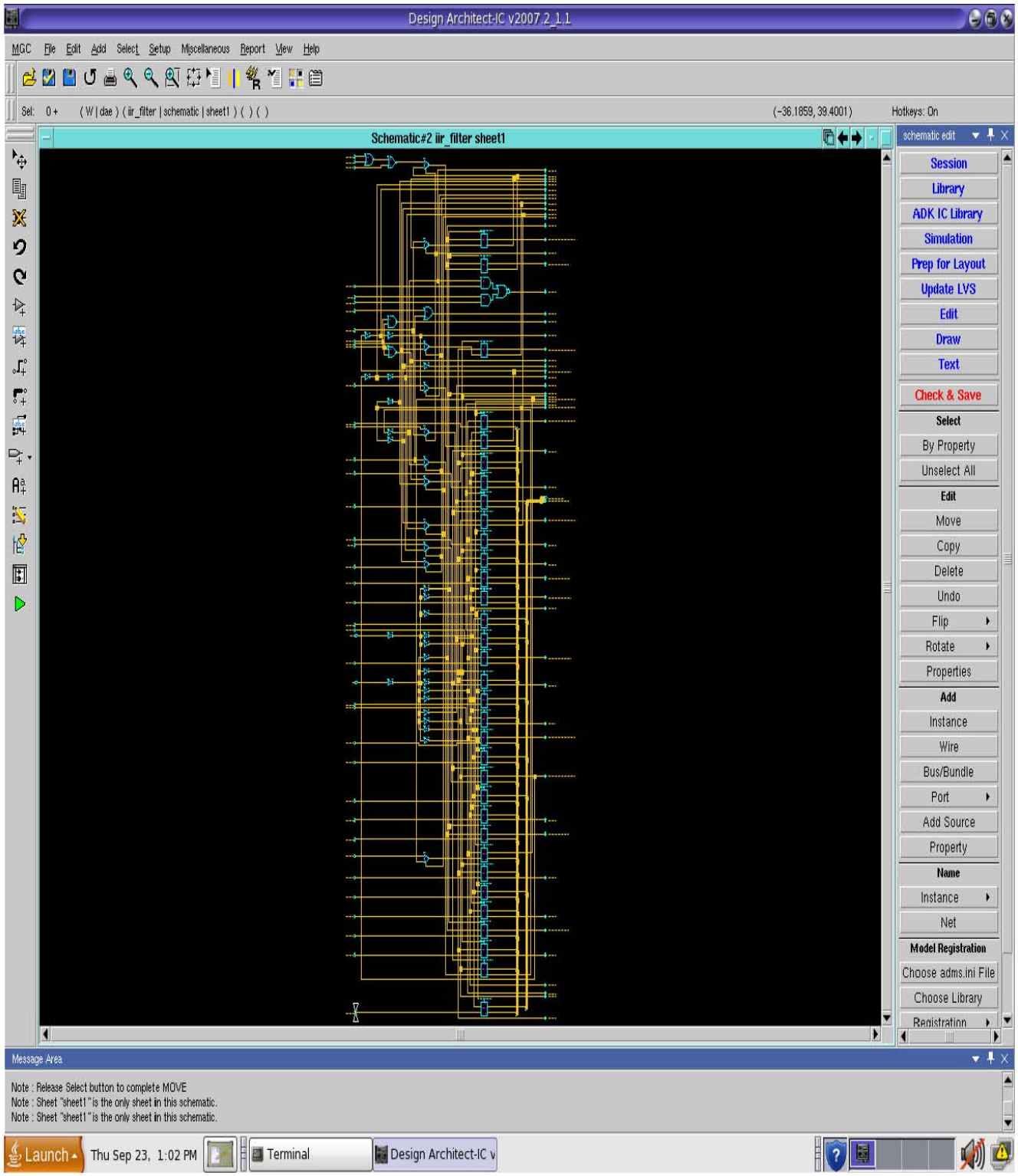

Figure 5.10: Gate level schematic of IIR filter Sheet#1 driven by transistors

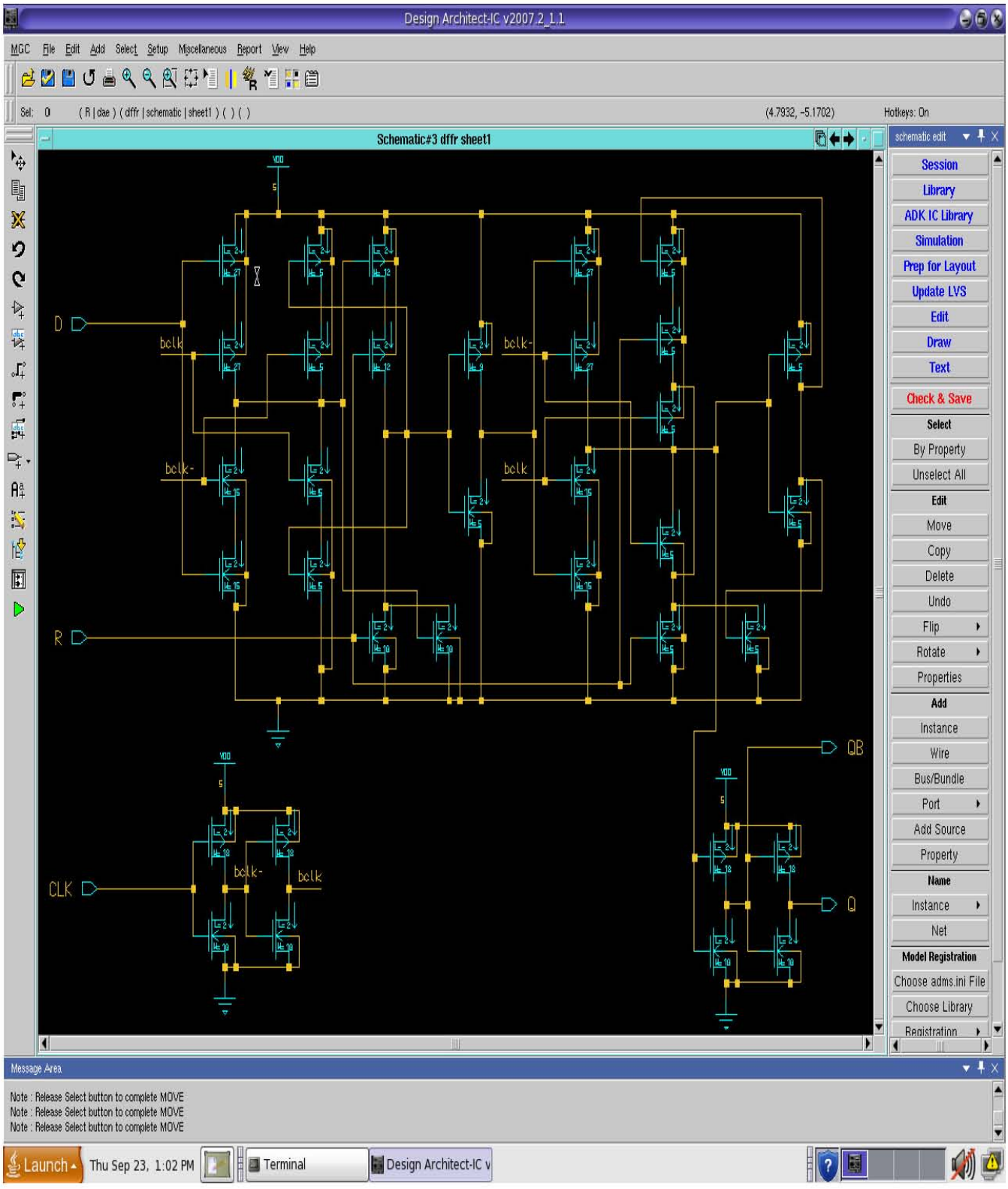

Figure 5.11: Transistor level schematic of DFF gate used in IIR filter schematic

5.4.1.6 Power Dissipation:

Power dissipation in CMOS IC's is due to the charging and discharging of capacitors this is the power that is converted to heat and then conducted or radiated away from the device. Circuits will draw different amount of current based upon the output of the gates.

A zero to one output transition draws energy from the power supply also a one to zero transition dissipates energy stored in CMOS transistor.
For example if Ic is the current drawn when all outputs are at logic zero & Is is the current drawn when all outputs are at logic 1.

So the average current drawn is Iavg = (Ic + Is)/2.

The average power dissipated can be calculated by:

P = Iavg*Vcc

The total power dissipation for IIR Filter design is 1.8097m WATT

Clock Frequency	No. of Gates	Power Dissipation	Slack
50Mhz	1673	1.8097mw	6.65ns

Table 5.1: Front End Design Specifications

5.4.2: Back End Design:

This is the lowest level of abstraction possible in circuit description. This process include steps like partitioning, floor planning, placements, routing, DRC, LVS, and generation of GDS-II which is submitted to foundry for chip fabrication. Before sending the GDS-II for mask preparation the design should be verified to confirm that there is no violation of any design rules, power and signal Integrity. In other words, a complete layout is designed and verified.

This is how the IC would look, if we took a closer look at it through the microscope. After the routing phase, Design rule checks and layout vs schematic checks are performed to verify layout block. Mentor Graphics IC-STATION tool is used for the layout design of IIR Filter.

5.4.2.1 Floor Planning:

A cell is created by specifying the technology and viewpoints. The most important part in a layout is floorplaining which gives a base line for a complete layout. Mentor Graphics Supports automatic floorplaining for the desired design. Figure 5.13 shows the floor plan for IIR Filter design.

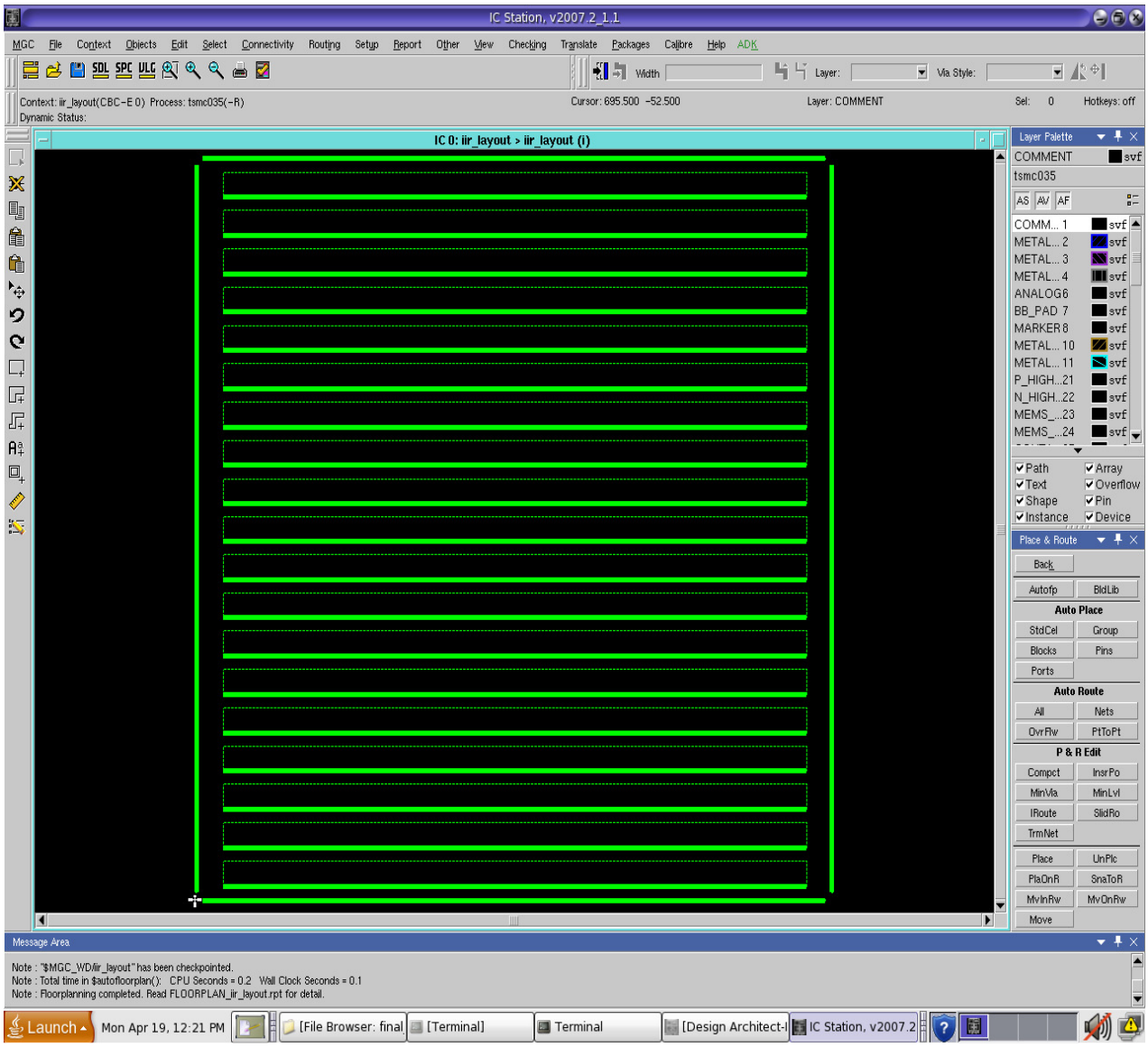

Figure 5.13: Floor Plan for IIR Filter Core cell

5.4.2.2 Placement of standard cells and ports:

After successful floor plan standard cells and ports are placed in a way that the routing should be easy to perform. Figure 5.14 shows the placement of standard cells. After placement port naming is performed the ports in layout are named according to the ports named in gate level schematic.

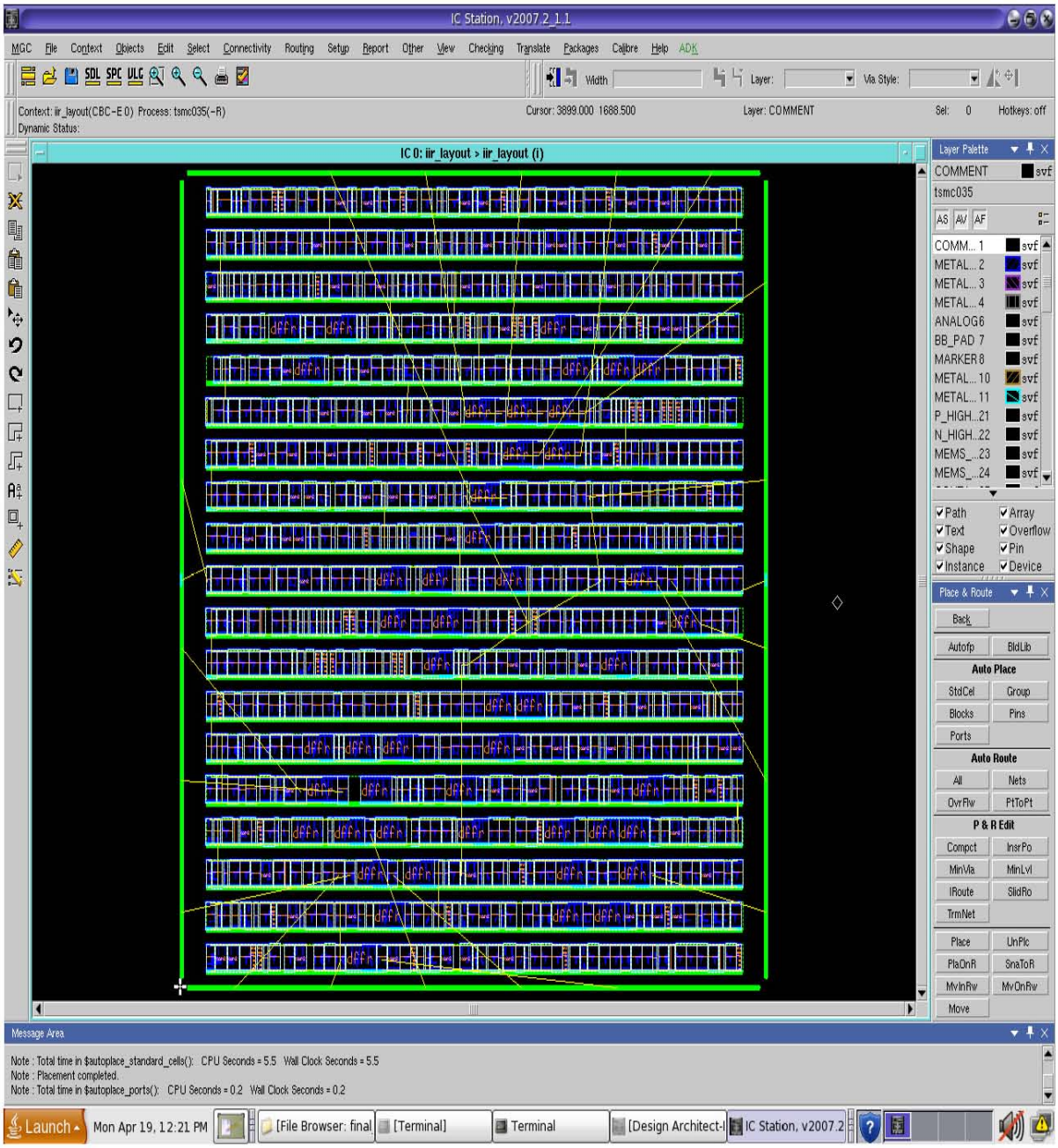

Figure 5.14: Standard cells and ports placement

5.4.2.3 Core Cell Complete Layout Design after Routing:

Mentor Graphic IC-Station support AUTO ROUTING which saves time for backend engineer. AUTO ROUTING does not perform routing completely many overflows are left behind. These overflows are routed manually to complete layout for the design. Figure 5.15 shows the complete layout design of IIR Filter core cell.

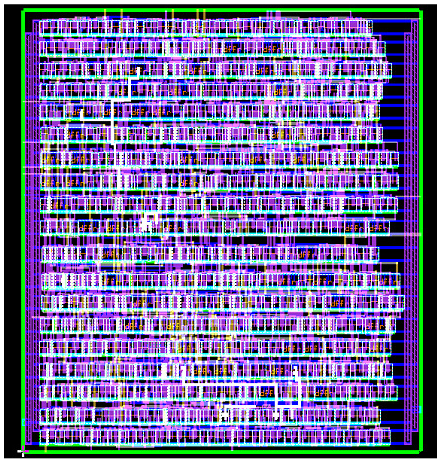

Figure 5.15: Core cell layout Design

Layers Used:

```
Layer Name
***************
METAL1.PORT
METAL2.PORT
METAL3.PORT
METAL4.PORT
VIA3
METAL4
P_WELL
N_WELL
ACTIVE
P_PLUS_SELECT
N_PLUS_SELECT
POLY
CONTACT_TO_POLY
CONTACT_TO_ACTIVE
METAL1
VIA
METAL2
VIA2
METAL3
METAL1_BLKG
METAL3_BLK
```

5.4.2.4 Core Cell Area:

From Figure 5.16 the core cell dimensions are obtained

X= 3493.468 Lambda

Y= 3796.000 Lambda

Feature size (F) = 0.35um

Lambda = F/2

= 0.175um

Area = X*Y = **0.406mm^2**

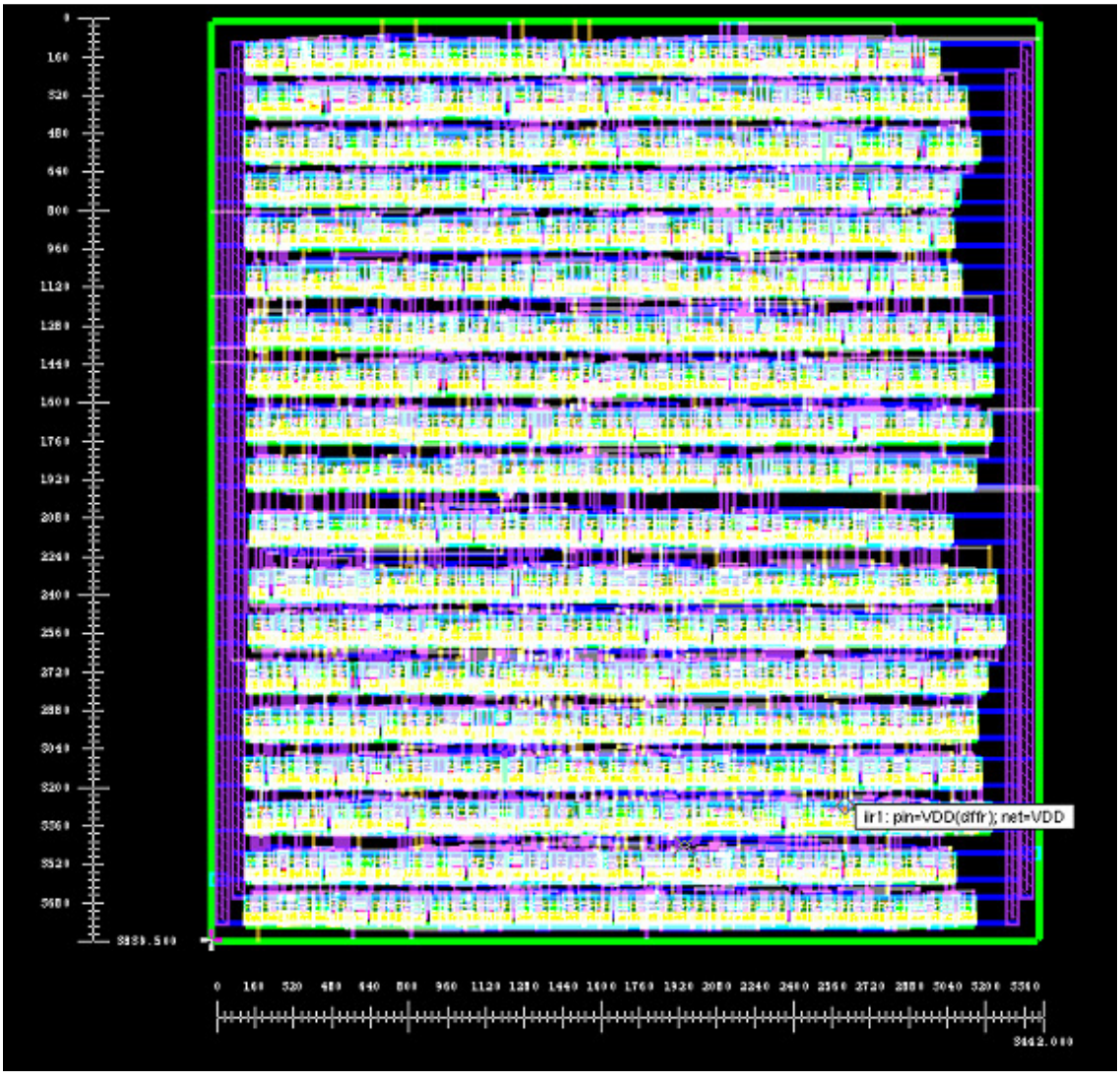

Figure 5.16: Core cell area

After this, Design rule checks and layout vs schematic checks are performed to verify layout block. Table 5.2 shows the complete backend design specifications.

5.4.2.5 Layout vs Schematic:

A Layout vs. Schematic (LVS) check is performed. This ensures that the layout is in conformance with the schematic. The design process moves back and forth between Layout, LVS and DRC. The LVS report generated from Mentor Graphics Calibre LVS is as follow:

```
                    CELL COMPARISON RESULTS (TOP LEVEL )

                          #       ###################       _   _
                        #         #                 #       *   *
                      #   #       #     CORRECT     #         |
                       # #        #                 #       \___/
                         #        ###################


LAYOUT CELL NAME:          iir_layout
SOURCE CELL NAME:          iir_filter

------------------------------------------------------------------------
INITIAL NUMBERS OF OBJECTS
--------------------------

                  Layout    Source          Component Type
                  ------    ------          --------------
 Ports:             21        21

 Nets:            4541      4539    *

 Instances:       4379      4379          MN (4 pins)
                  4382      4379    *     MP (4 pins)
                  ------    ------
 Total Inst:      8761      8758


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                  Layout    Source          Component Type
                  ------    ------          --------------
 Ports:             21        21

 Nets:            2121      2121

 Instances:         65        65          MN (4 pins)
                   435       435          MP (4 pins)
```

```
                      8          8          SDW3 (4 pins)
                      1          1          SUP3 (4 pins)
                    386        386          SPDW_2_1 (4 pins)
                     36         36          SPDW_2_2 (5 pins)
                      1          1          SPDW_3_2_1 (7 pins)
                     16         16          SPUP_2_1 (4 pins)
                     37         37          SPUP_2_2 (5 pins)
                      7          7          SPUP_3_2 (6 pins)
                      1          1          SPUP_3_2_1 (7 pins)
                    786        786          _invv (4 pins)
                     23         23          _invx2v (4 pins)
                    418        418          _nand2v (5 pins)
                      5          5          _nand3v (6 pins)
                      8          8          _nand4v (7 pins)
                    180        180          _nor2v (5 pins)
                      9          9          _nor3v (6 pins)
                    440        440          _sdw2v (4 pins)
                    801        801          _smp2v (4 pins)
                 ------     ------
 Total Inst:      3663       3663

   * = Number of objects in layout different from number in source.
```

5.4.2.6 Design Rules Check:

This stage is often dependent on the final process technology that is used to manufacture the Chip. The design rule check ensures that the rules laid down by the fabrication process technology are not violated. A good example would be some processes need transistors, wires and polysilicon to be of a certain minimum width. The layout would have to be drawn based on such constraints. Mentor Graphics Calibre DRC is used for this purpose and Figure 5.17 shows the Calibre DRC verification.

The design toggles between Layout, LVS and DRC. The DRC results are shown in figure 5.17.

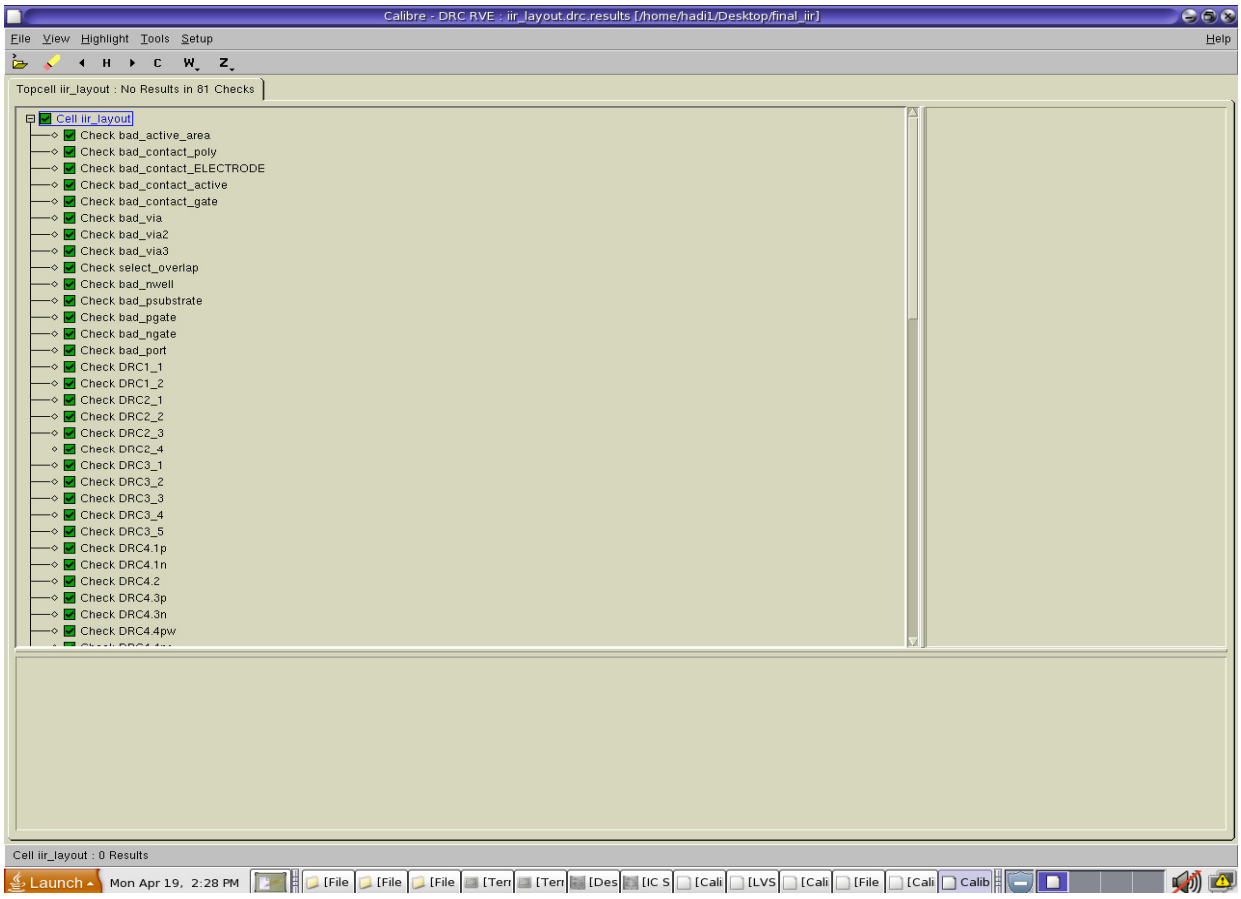

Figure 5.17: Design Rules Check

Nmos Transistors	Pmos Transistors	Total no. of transistors	Core Cell Area
4379	4379	8758	0.406mm^2

TABLE 5.2: Back End Design Specifications

5.4.3 Pads Placement:

This is the final stage in which the pads are first placed at the schematic end by using Design Architect tool Figure 5.18 shows the pads placement.

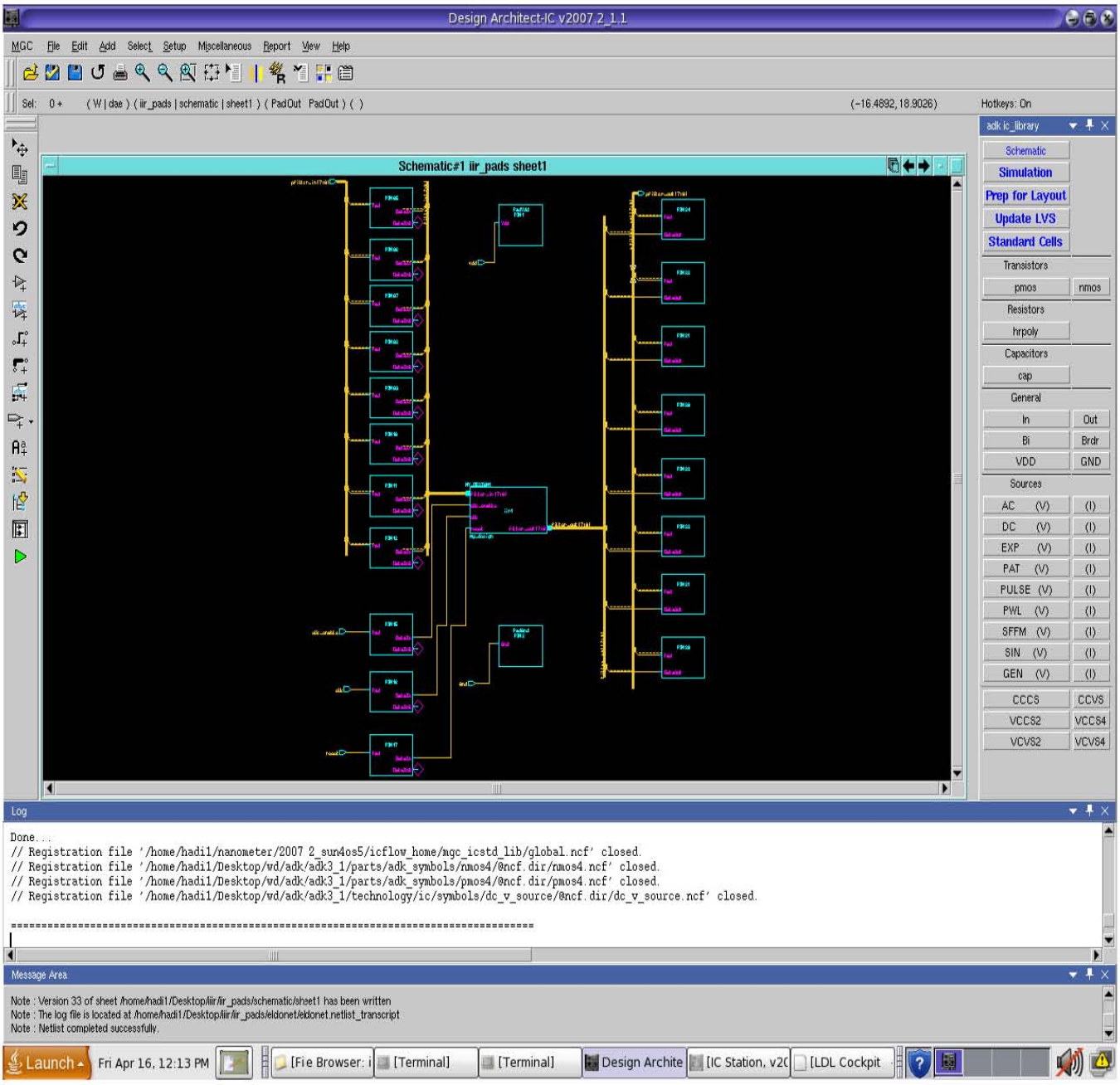

Figure 5.18: Pads Placement in Schematic

View points are again created and final chip design for IIR Filter is completed Figure 5.19 shows the complete chip design for memory efficient IIR filter.

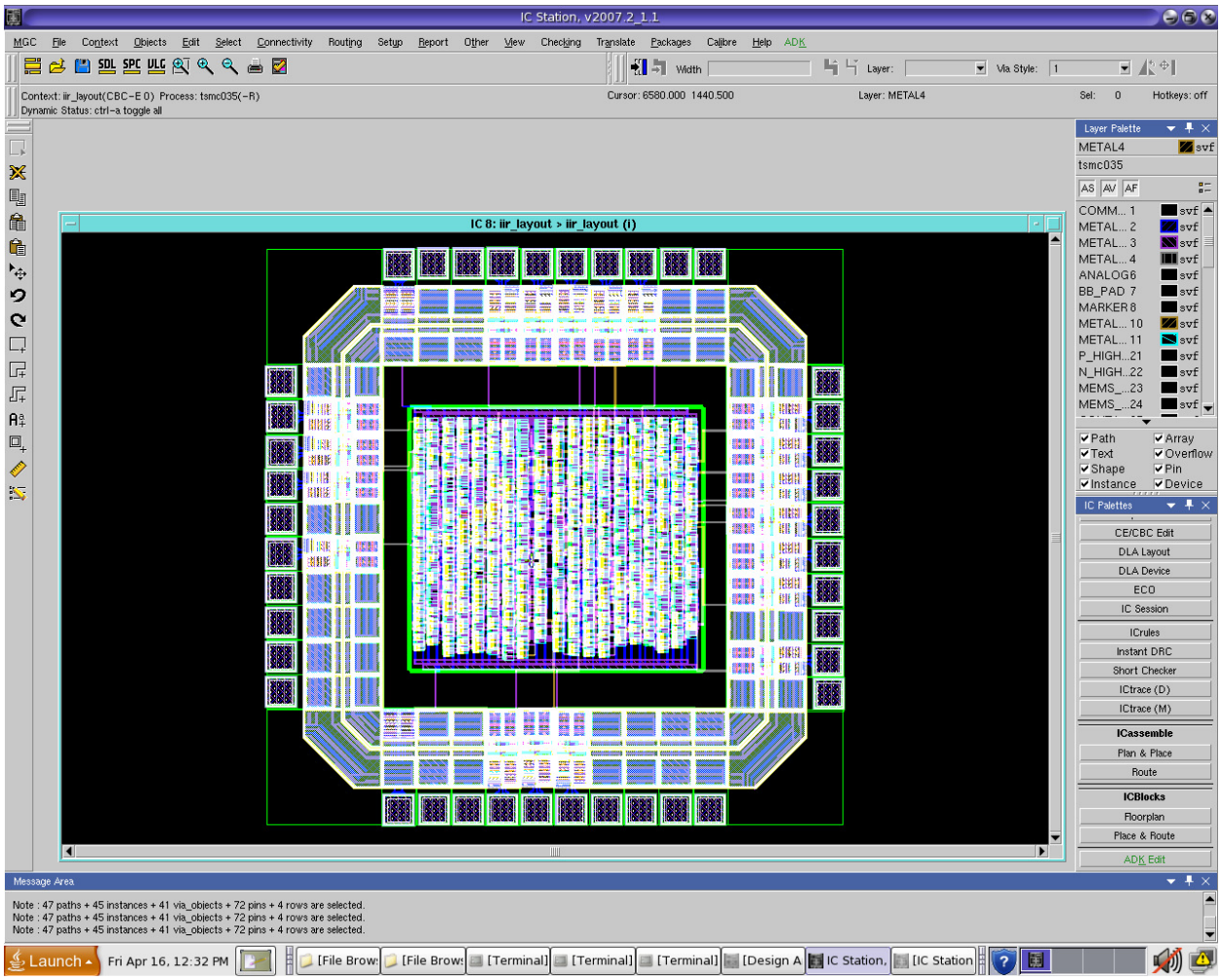

Figure 5.19: Final Chip Design of IIR Filter

5.4.4 GDS II:

This is the final stage before fabrication. Fabrication plants accept submissions GDS II format. These are computer generated files that describe the IC layout. They incorporate all the necessary details for manufacturing the chip.

Chapter 06

Conclusion and Future Work

6.1 Conclusion:

We have presented a memory efficient IIR equalizer which halves the memory requirement of the conventional design. Both equalizer designs are characterized in context of UWB prolate spheroidal wave signaling function (PSWF) having duration of 0.15ns, which were transmitted every 120 ns as in [18], [19]. We obtain exactly the same BER performance as in [18], [19]. The memory efficient IIR equalizer was modeled in HDL for implementing the design on ASIC using a Mentor Graphics IC design flow which provides an extra level of verification using post synthesis simulation technique at gate level. The front end and back end design was completed and verified successfully using TSMC 0.35um technology up to GDS II format which could be fabricated and used as an independent chip to equalize the distortion effects in UWB channel.

6.2 Future Work:

The future work includes the fabrication of memory efficient IIR filter chip this involves coordination with MOSIS to come up with a physical chip. After fabrication this chip can be used in educational as well as industrial environment which can help in reducing the distortion effects occurred in UWB channel in an efficient way.

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