## HARDWARE PROGRAMMING OF FEED FORWARD NEURAL CONNECTIONIST NETWORK



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A thesis submitted in fulfilment of the requirements for the award of the degree of Master of Science (Computer Engineering)

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## THESIS COMPLETION CERTIFICATE

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I, SYED SHABBAR ALTAF hereby declare that I have written this thesis titled as "Hardware Programming of Feed-Forward Neural Connectionist Network" based on my efforts under the sincere guidance of my supervisor Dr Khalid Javed and seniors who have worked as pioneers in the field. All citations with references to all sources used in this thesis have been mentioned clearly. I certify that this work contains no material which has been submitted for the award of any thesis or any published material except where due references have been made in the text.

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I solemnly declare that research work presented in the thesis titled "Hardware Programming of Feed-Forward Neural Connectionist Network" is solely my research work with no significant contribution from any other person. Small contribution / help wherever taken has been duly acknowledged and that complete thesis has been written by me.

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I would like to dedicate this thesis to my loving parents, my wife and pieces of my heart my sweet sons . . .

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#### **ABSTRACT**

This thesis deals with a top-down design methodology of a connectionist neural network-based upon parametric Verilog HDL description. To come off early in the design process, a high regular architecture was achieved. Then, the Verilog HDL parametric description of the network was realized. The description is the building block of the architecture and has advantages such as generic, flexible and could be easily modified as the dictates of user requirements. Hardware programming of the connectionist neural network becomes very interesting due to re-programmability features of application tools such as FPGA circuits. More precisely, the Verilog HDL based synthesis tools have become very popular due to the need-driven approach of today, to get a correctly working system in the first place. Moreover, the system has to be technology independent design having the capability of design reusability, the ability to experiment with several alternatives of the design, and economic factors such as time to market.

To this aim, the digital implementation of Feed-Forward Connectionist Network is proposed in this thesis using Verilog HDL synthesis tools. A new design methodology of ANNs based upon Verilog HDL synthesis of the network will be applied. The proposed architecture can be used in different Machine Learning applications such as Classification, Controls, Estimation, and Prediction, etc. The proposed methodology, however, is mainly focused on the Classification application and its illustration while using the FPGA as a tool. Further, the design is capable enough to be modified based on the dictates of the user requirements for any specific project proposed to achieve the results in the used cases in hand. The implementation of Feed-Forward Connectionist Network could then be driven from this as a take-off platform for subsequent development carefully tailored to meet the user demands.

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